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ElectronicsWeek®

NOVEMBER 19, 1984 $3

9 DEC REC'D

Cheap chips prevent overvoltage

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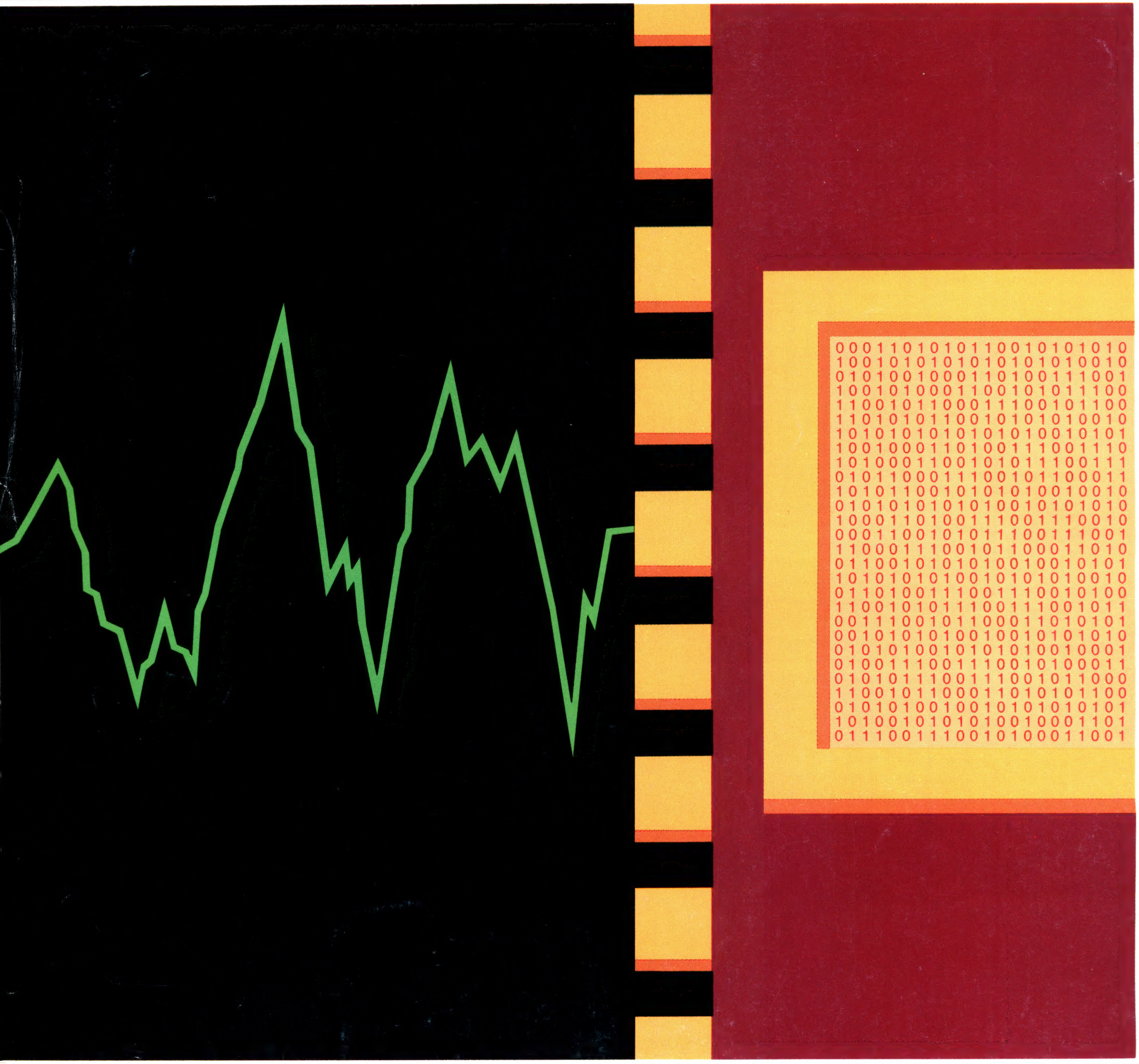

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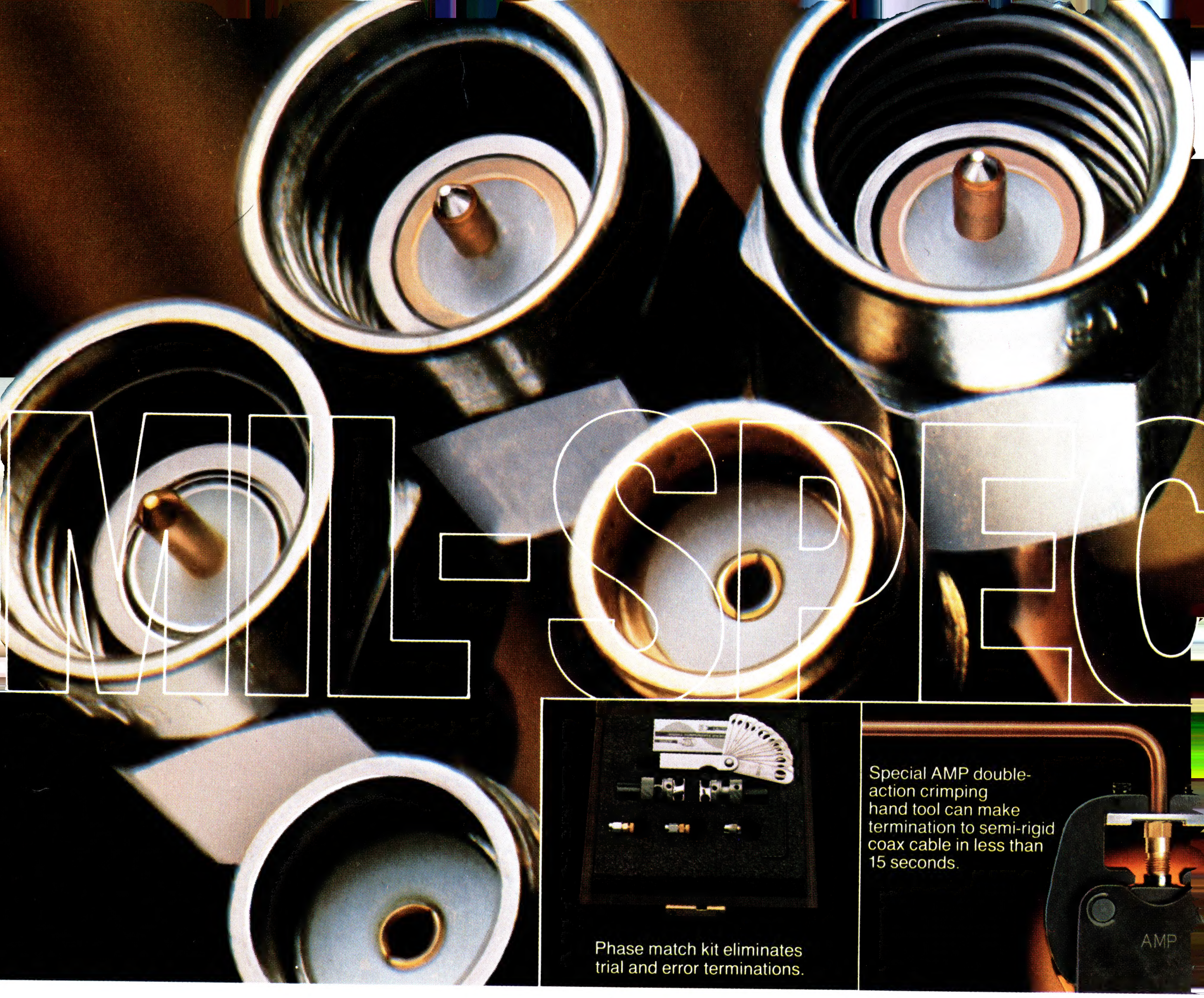

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Next ElectronicsWeek

CMOS is pushing n-MOS out of the big-memory picture

With n-MOS running out of steam as a workable memory technology—for example, in dynamic random-access memories, the limit seems to be 256-K—the consensus among semiconductor executives is that CMOS is getting to be the big kid on the block. In high-speed static RAMs, the transition point is at the 4-to-16-K level; in medium-speed SRAMs, 16-to-64-K; in masked read-only memories, 1-to-4-Mb; for programmable ROMs, 512-K-to-1-Mb; and in electrically erasable PROMs, 32-to-64-K. Examine the details of the changes as well as the significance of the evolution in a special report appearing in next week's *ElectronicsWeek.*

Acoustic microscopes: the latest test tool

Acoustic microscopes give makers of chip capacitors and hybrid microelectronic circuits the ability to test chips for internal defects, such as cracks, rapidly and nondestructively. With magnification capabilities ranging from 7× to 400×, these instruments resemble more common light microscopes but offer the advantage of extreme sensitivity to internal discontinuities, both in light-transparent and light-opaque materials. Read about acoustic microscopes in next week's *ElectronicsWeek.*

Looking ahead in ElectronicsWeek

The world of information technology is waiting eagerly to find out what the Japanese are doing in their fifth-generation computer project. What progress has been made during the initial three-year-long research and development phase of the 10-year project? Computers Editor Tom Manuel has just returned from Tokyo and the International Conference on Fifth Generation Computer Systems 1984, at which the Japanese reported on their progress. He'll have a complete report in an upcoming issue.

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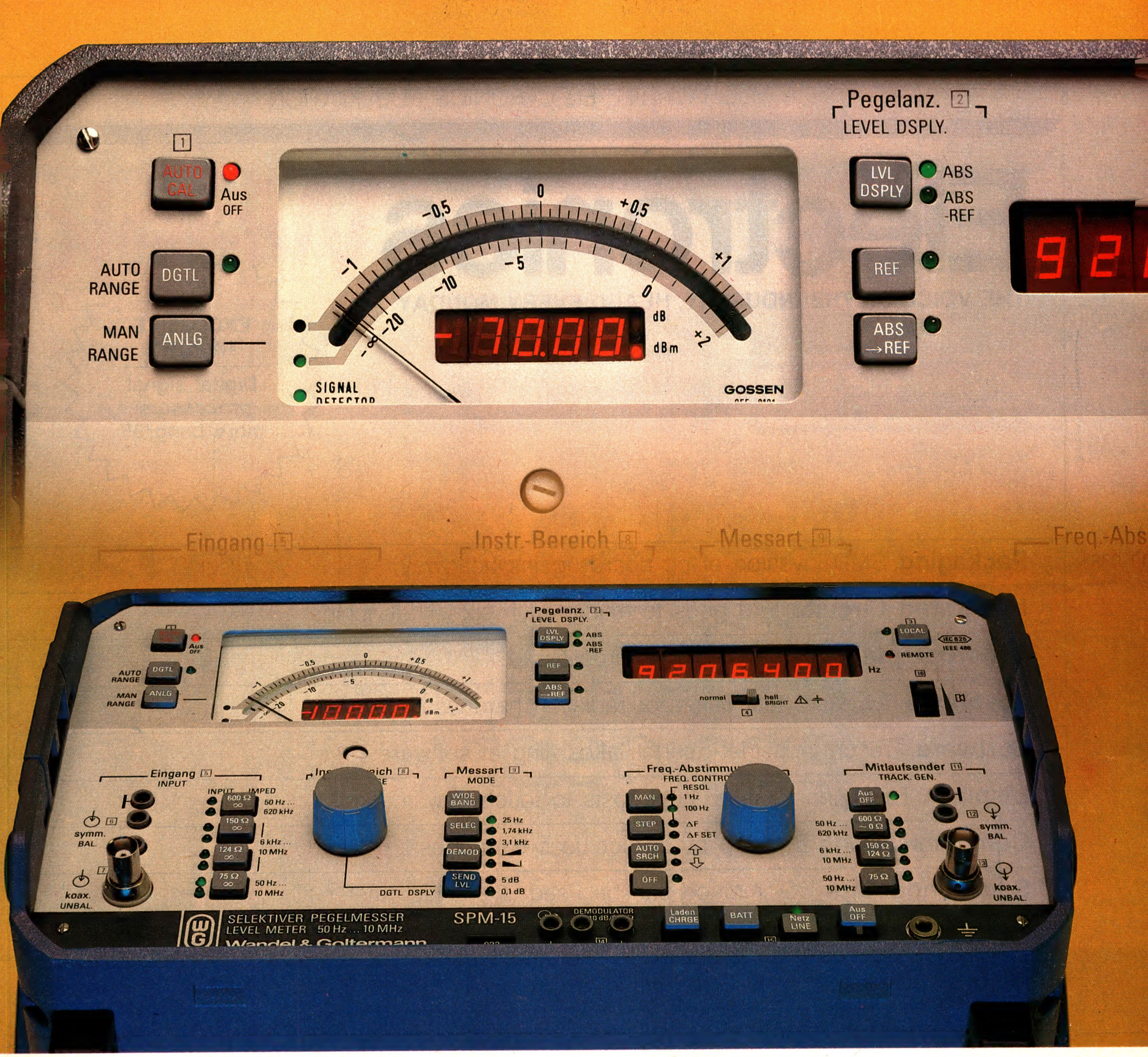

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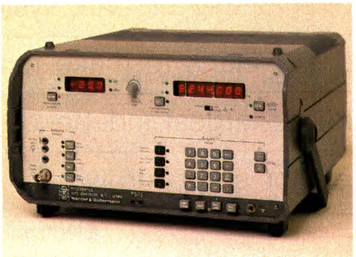

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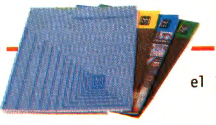

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THE VOICE OF THE INDUSTRY, HEARD EVERY MONDAY

EXCLUSIVE REPORT

Digital signal processors: more bang/65

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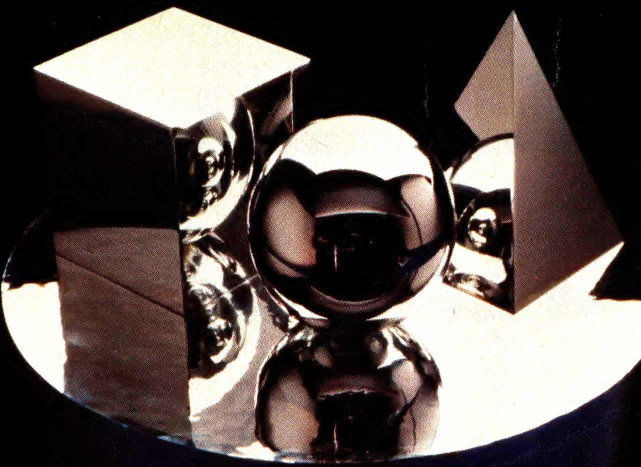

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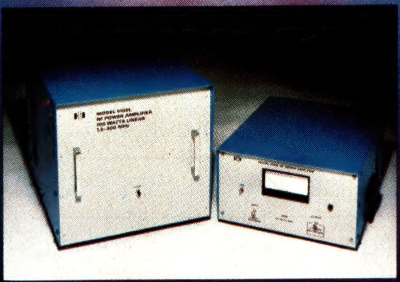

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ElectronicsWeek

Special Technology Reports

DSPs Digital signal processors: Doing more with less.
Chip makers are drawing a parallel between DSPs and the microprocessor. "What a micro was to logic, a digital signal processor is to analog," says one. It appears that the applications possibilities for DSPs are about to explode **65**

Systems designers find answers in digital signal processing **66**

Semiconductors Flexx arrays speed IC design.
The new Flexx array approach to the design of integrated circuits keeps the advantages of both gate arrays and standard cells but eliminates many of their drawbacks. The technique is technology independent, available today in Schottky logic and soon in CMOS **71**

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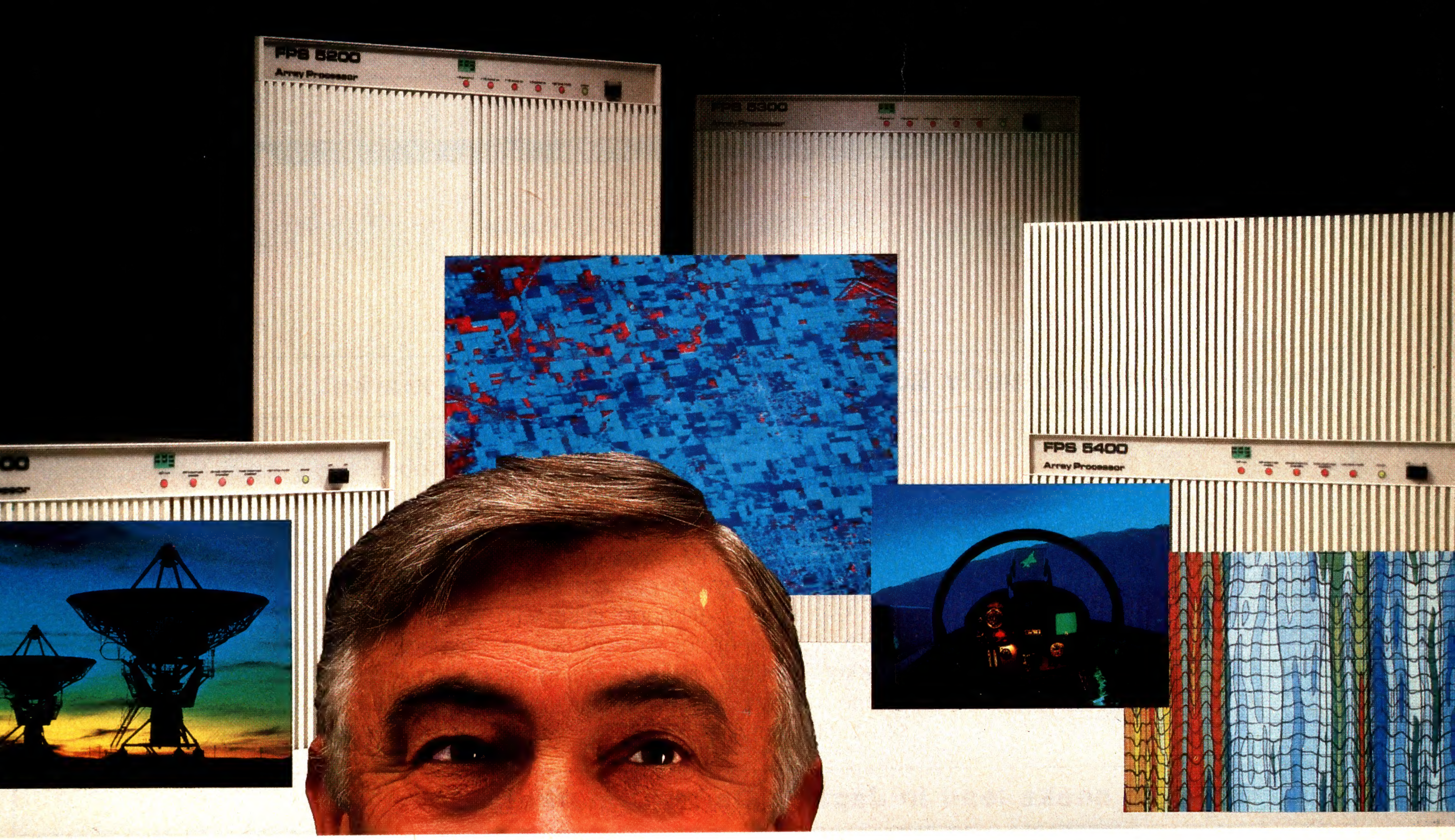

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UP FRONT

Talks underway to unify European switching-equipment market

Talks now under way could eventually unify 70% of Europe's telecommunications switching-equipment market. In October, Italy's Italtel SpA signed an accord with France's CIT-Alcatel to engage in joint research and development work on compatible electronic exchange components. The two companies want to extend that agreement to include West Germany's Siemens AG and the UK's Plessey Co. plc. Agreement with Siemens could be reached as early as next spring, although talks with Plessey are apparently less advanced. Such a four-partner accord would create a "telecommunications common market," sources believe, giving each partner the opportunity to specialize in home markets and the power to compete in export markets with non-European multinationals.

GigaBit Logic seeks lead in Japan's GaAs IC market

GigaBit Logic Inc. is trying to become the market leader in digital gallium arsenide integrated circuits in Japan. The Newbury Park, Calif., company has started sampling 70 kinds of high-speed products, including 1-K static random-access memories and logic products, through Tokyo Electron Ltd. [*ElectronicsWeek,* Nov. 5, 1984, p. 56]. In about six months, Tokyo Electron plans to start volume sales of the products, with particular emphasis on the products that prove most popular during the sampling period. Japanese semiconductor companies have fabricated GaAs memory chips, gate arrays, and multipliers on an experimental basis, but so far none has commercial digital products on the market.

Semiconductor book-to-bill level drops to lowest level in six years

The semiconductor business continued to suffer last month, as the industry's closely watched book-to-bill ratio fell yet again—slipping to 0.67:1, the lowest figure in six years, according to the Semiconductor Industry Association, San Jose, Calif. The ratio, which indicates the dollar value of new orders versus the value of products shipped, has been declining steadily this year. In September, it dropped to 0.84:1, the first time in 18 months that it fell below 1:1. The decline indicates continued widespread inventory adjustment among electronics-equipment manufacturers. The monthly average of orders fell 22% in October, to $694 million from September's $893 million.

Intel Corp. shouldn't be too unhappy with the decline, though. The Santa Clara, Calif., firm just received a $31 million order from distributor Hamilton-Avnet, of Culver City, Calif., for 256-K dynamic random-access memory chips. Shipments of the chips, which Intel has been producing since June using its C-H-MOS process, will begin immediately.

DOD gives $103 million to Carnegie-Mellon for software institute

The Department of Defense has awarded Pittsburgh's Carnegie-Mellon University funding to the tune of $103 million over the next five years to build and staff a Software Engineering Institute. A university representative says that the institute, to be located near the university's campus, would work on improving the reliability and capability of systems software for the military. The institute will draw on the faculty and software work in progress at Carnegie-Mellon's computer science department and will eventually have 250 high-level positions, the representative says.

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- *soft recovery*
- *low forward voltage drop.*

$V_{RRM} = 200, 300$ and $400\,V$
ultra-fast free wheel diode
t_{rr}: from 25 to 50 ns max.
$V_F/I_0 = 1.4\,V$

$I_{F(AV)}$	CASE TYPE	NON INSULATED CASE	INSULATED CASE
1 A	F 126	BYT 01	
3A	DO 27	BYT 03	
8A	DO 220	BYT 08 P	BYT 08 PI*
12A	DO 4	BYT 12	
16A (2 x 8)	TO 220	BYT 16 P	
30A	DO 5 DOP 3	BYT 30 BYT 30 P	BYT 30 PI*
60A	DO 5 DOP 3	BYT 60 BYT 60 P	
60A (2 x 30)	ISOTOP		BYT 230 PI*

*Insulating voltage: 2500 VRMS

$V_{RRM} = 600, 800\,V$
ultra-fast free wheel diode
t_{rr} max. $\leqslant 60\,ns$
$V_F/I_0 = 1.7\,V$

$I_{F(AV)}$	CASE TYPE	NON INSULATED CASE	INSULATED CASE
12A	DO 4 DO 220	BYT 12 BYT 12 P	**BYT 12 PI***
30A	DO 5 DOP 3	**BYT 30** BYT 30 P	**BYT 30 PI***
60A (2 x 30)	ISOTOP		**BYT 230 PI***

*Insulating voltage: 2500 VRMS

$V_{RRM} = 1000\,V$
ultra-fast free wheel diode
t_{rr} max. $\leqslant 70\,ns$
$V_F/I_0 = 1.8\,V$

$I_{F(AV)}$	CASE TYPE	NON INSULATED CASE	INSULATED CASE
12A	DO 4 DO 220	**BYT 12** **BYT 12 P**	**BYT 12 PI***
30A	DO 5 DOP 3	**BYT 30** **BYT 30 P**	**BYT 30 PI***
60A (2 x 30)	ISOTOP		**BYT 230 PI***

*Insulating voltage: 2500 VRMS

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- *low forward recovery time, t_{fr}: from 10 to 20 ns.*

$V_{RRM} = 50, 100, 150, 200\,V$
t_{rr}: from 25 to 50 ns max.
$V_F/I_0 = 0.85\,V$

$I_{F(AV)}$	CASE TYPE	NON INSULATED CASE	INSULATED CASE
1 A	F 126	BYW 100	
3A	DO 27	BYW 98	
7A	DO 220	BYW 80	
15A	DO 4 DO 220	BYW 81 **BYW 81 P**	**BYW 81 PI***
20A (2 x 10)	TO 220	BYW 51	
25A	DO 4 DOP 3	BYW 77 **BYW 77 P**	**BYW 77 PI***
30A (2 x 15)	TOP 3	**BYW 99 P**	
35A	DO 5	BYW 92	
50A	DO 5	BYW 78	
60A (2 x 30)	TOP 3	BYV 52	
80A	DO 5	BYW 08	
100A (2 x 50)	ISOTOP		BYV 54*

*Insulating voltage: 2500 VRMS

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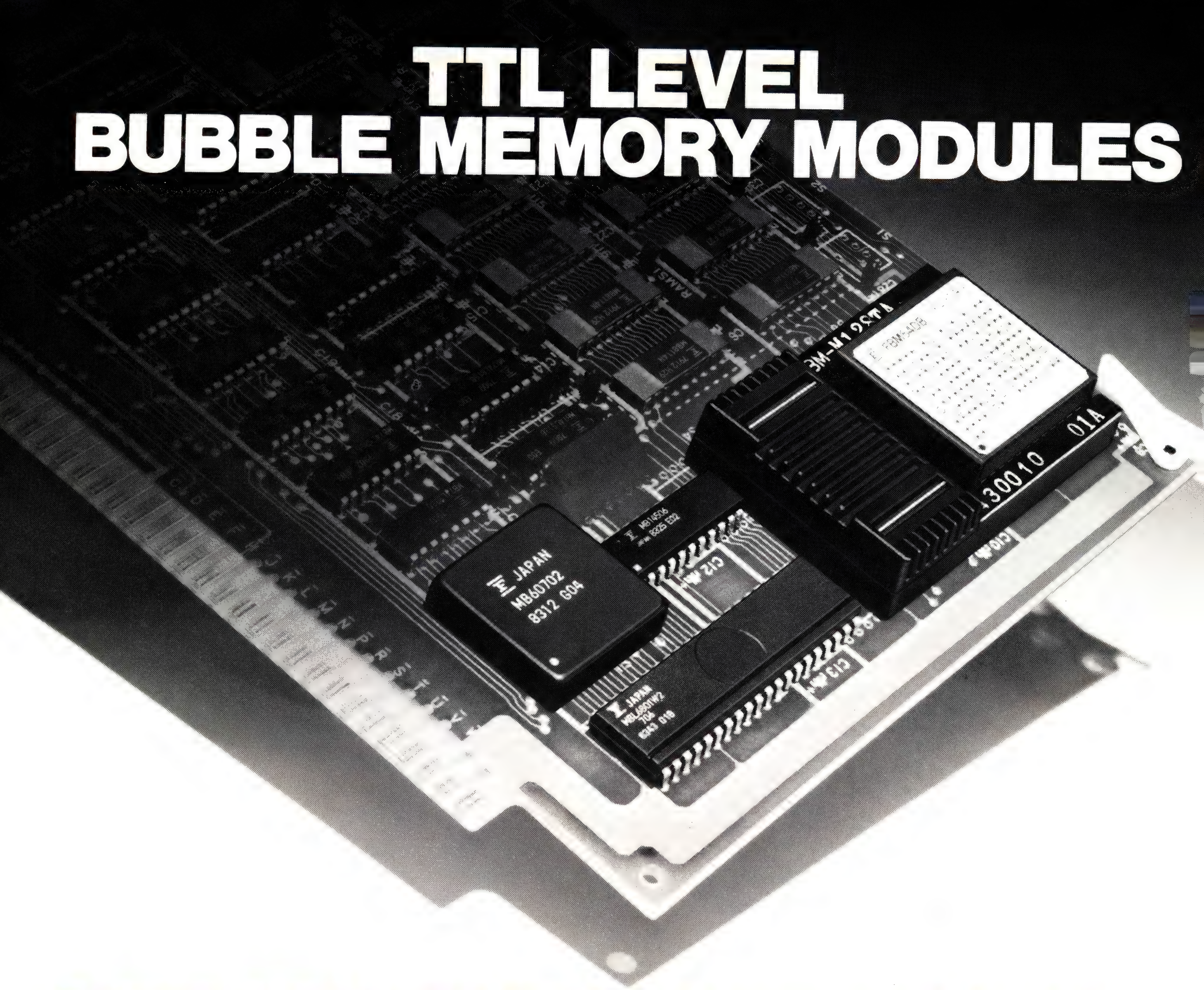

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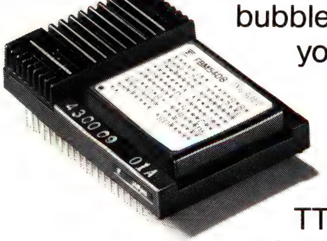

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- ●Non-volatile memory
- ●Maintenance-free design

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Model	FBM-M128TA	FBM-M128TC
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Interface	TTL level	
Transfer rate	100K bit/s	
Access time	11.2ms	
Operating temp.	0 to 65°C	5 to 50°C
Storage temp.	–40 to 85°C	–30 to 75°C
Weight	75g	
Dimensions	43.5 x 65.5 x 13.7mm	

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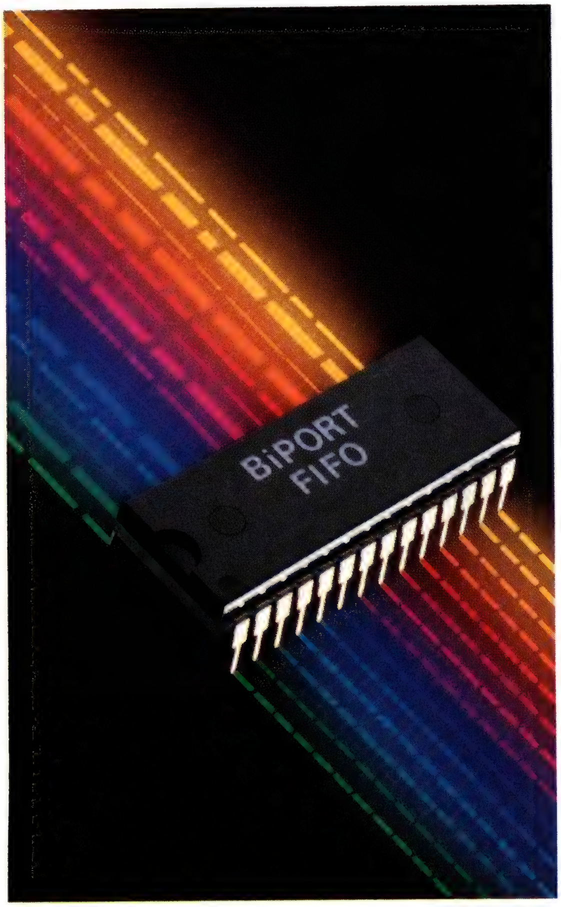

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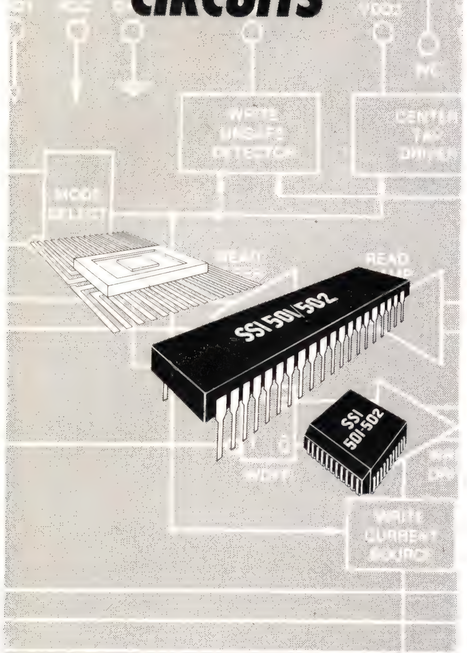

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Meetings

Com-Struct '85, Slater Publications Inc. (Com-Struct '85, 163 Highland Ave., Needham Heights, Mass. 02194), Bayside Exposition Center, Boston, Jan. 8-10.

IC Assembly Automation Conference, Intem Show Management (Malka Nagel, Intem Show Management, P.O. Box 390207, Mountain View, Calif. 94039), Le Baron Hotel, San Jose, Calif., Jan. 9-10.

Telecommunications for Pacific Development: Toward a Digital World, Pacific Telecommunications Council (1110 University Ave., Suite 308, Honolulu, Hawaii 96826), Sheraton-Waikiki Hotel, Honolulu, Jan. 13-16.

Advances in Display Technology V, Society of Photo-Optical Instrumentation Engineers (SPIE, P.O. Box 10, Bellingham, Wash. 98227-0010), Los Angeles Marriott Hotel, Los Angeles, Jan. 20-25.

Advanced Semiconductor Equipment Exposition & Technical Conference, Cartlidge & Associates (Joyce Estill, Cartlidge & Associates Inc., 1101 S. Winchester Blvd., #M259, San Jose, Calif. 95128), San Jose Convention Center, San Jose, Calif., Jan. 22-24.

Third International Modal Analysis Conference, International Society for Modal Testing and Analysis and Union College (Peter B. Juhl, Union College, Graduate and Continuing Studies, 1 Union Ave., Schenectady, N.Y. 12308), Orlando Marriott Inn, Orlando, Fla., Jan. 28-31.

Communication Networks Conference & Exposition, Conference Management Group (CW/Conference Management Group, 375 Cochituate Rd., Box 880, Framingham, Mass. 01701), Washington Convention Center, Washington, Jan. 28-31.

Industrial Productivity Conference and Exposition, Society of Manufacturing Engineers (1 SME Dr., Dearborn, Mich. 48121), Expo Centre, Orlando, Fla., Jan. 29-31.

Micro-Computer '85, Messe Frankfurt Ltd. (Philippe Hans, German American Chamber of Commerce, 666 Fifth Ave., New York, N.Y. 10103), Frankfurt Fairgrounds, Frankfurt, Jan. 29-Feb. 3.

Aerospace Applications Conference, IEEE (Russell Gaspari, Hughes Aircraft, MS S12/W315, P.O. Box 92919, Los Angeles, Calif. 90009), Snowmass, Colo., Feb. 2-9.

1985 Office Automation Conference, American Federation of Information Processing Societies Inc. (1899 Preston White Dr., Reston, Va. 22091), Georgia World Congress Center, Atlanta, Feb. 4-6.

Fourth Middle East Communication Show, Kallman Associates (5 Maple Ct., Ridgewood, N.J. 07450), Bahrain, Feb. 4-7.

Mini/Micro West, IEEE and ERA (Electronic Conventions Management Inc., 8110 Airport Blvd., Los Angeles, Calif. 90045), Anaheim Hilton Exposition Center, Anaheim, Calif., Feb. 5-7.

Stride Faire '85, Stride Micro (4905 Energy Way, Reno, Nev. 89502), MGM Grand Hotel, Reno, Nev., Feb. 8-10.

Optical Fiber Communication Conference, IEEE (Optical Society of America, 1816 Jefferson Place N.W., Washington, D.C. 20036), Town & Country Hotel, San Diego, Feb. 11-13.

Seminar

Data Base Design, Data General Corp. (Data General, Educational Services Department, Mail Stop F019, 4400 Computer Dr., Westboro, Mass. 01580), Data General Customer Education Center, Dallas, Jan. 16-18.

Tape Automated Bonding; Injected Molded Plastic Substrates, International Organization of Professional Advancement Conferences (59 N. Santa Cruz Ave., Suite Q, Los Gatos, Calif. 95030), Newport Marriott, Newport Beach, Calif., Jan. 21.

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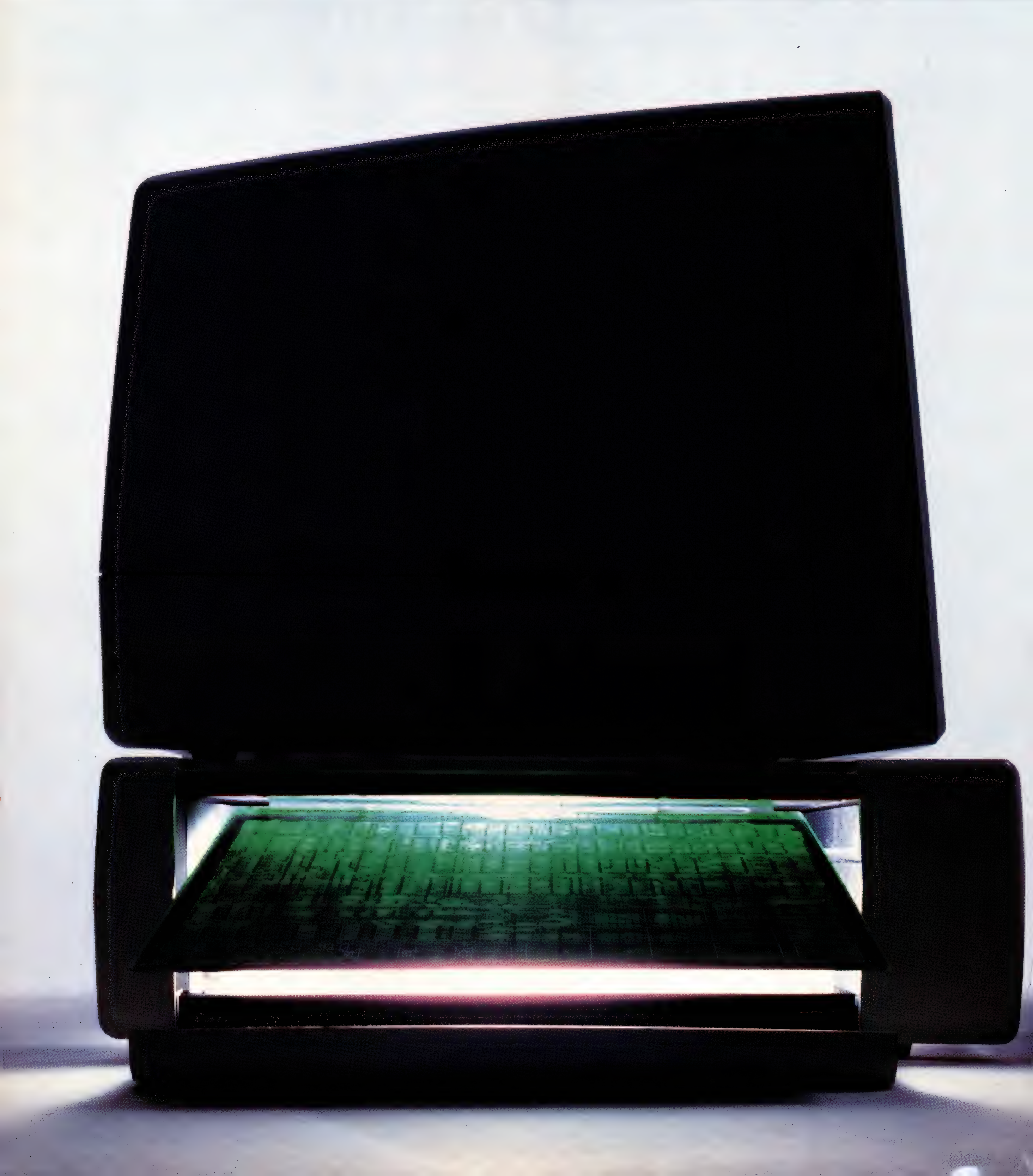

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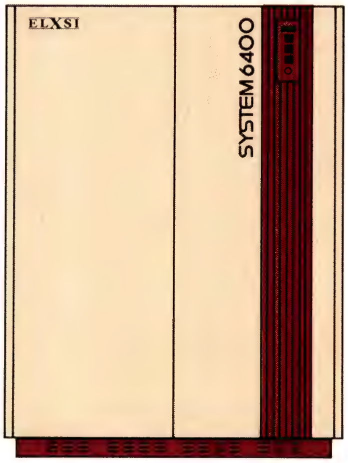

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Circle 16 on reader service card

SMD INVASION OF PC BOARDS GAINS HEADWAY

Components makers and systems houses want to be through with through holes, but standards are lacking ☐ *By J. Robert Lineback*

Colorado Springs, Colo.

The revolution that surface-mounted devices (SMD) have brought to semiconductor packaging has turned the use of small, passive components into anything but a trivial pursuit for competitive players in the printed-circuit-board game.

Space-saving SMDs and their associated assembly-line automation have left many eager systems houses puzzled over each and every piece of a new pc-board design. Choices appear greatest in the passive-components arena, where producers of widely used device types are attempting to set *de facto* industry standards for what is eventually expected to be huge volumes of surface-mountable products. Consequently, the large—but plodding—passive-components industry has suddenly become an active business.

Hurry-up meeting. Because of concern over the scramble to shape standards, the Electronic Industries Association has called for a winter forum; its fear is that U.S. systems firms are slipping behind foreign competitors in adopting next-generation packaging concepts. Dubbed Smart—for Surface Mount and Reflow Technology—the meeting is slated for Jan. 14-16 in New Orleans. It is being designed to bring together a wide range of U.S. components producers, customers, and production-equipment suppliers; the meeting will cover both the economics and technology of SMDs (the basic fee is $200 for EIA members).

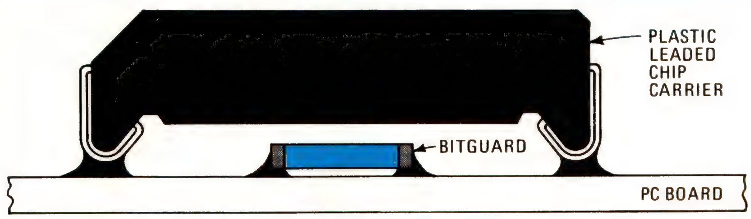
"We are making a mass mailing and think people will flock to the meeting if they know about it," states Mark Donovan, who heads up the project for the EIA's Compo-

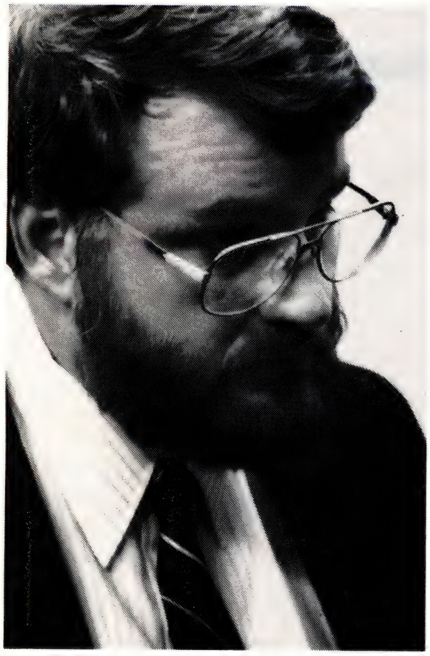
Chip capacitor slips under SMD

Something new has emerged from the surface-mounting efforts at AVX Corp. It's a new line of decoupling multilayer ceramic capacitors that fit snugly beneath dynamic memories housed in plastic J-leaded chip carriers. After nearly two years of work, AVX has developed a proprietary manufacturing process that minimizes warpage of barium-titanate dielectric material. The sintering process often makes the multilayer ceramic material curl up, but AVX's new process holds the thickness to between 15 and 18 mils, says John Maxwell, marketing manager for advanced decoupling products at the company's Colorado Springs facility.

Maxwell says the 120-by-100-mil surface-mounted BitGuard capacitor is being used by Texas Instruments Inc. to reduce the size and improve yields on single in-line package modules containing 64-K dynamic random-access memories. Compared with placement alongside RAMs, the capacitor under the plastic leaded chip carrier saves between 10% and 15% of board space, he says. By placing the component under the RAM chip carrier, SIP memory-module makers can also avoid mounting devices on both surfaces of the motherboard, which can reduce yields. "When you have a thin part and you are hiding it under the chip carrier, warpage figures become very important," notes Maxwell. Surface-mounted BitGuard capacitors have been optimized for 64-K and 256-K DRAMs.

Engineers exploring SMD packages have also developed another space-saving concept: placing bare DRAM dice on top of decoupling capacitors. This saves an additional 20% to 30% of space, says Maxwell. Dice are fixed to the capacitor with a conductive glue. "Basically, it's an insulating shelf that the memory die sits on," he explains. —**J.R.L.**





Teach and learn. John Maxwell, who oversees AVX Corp.'s surface-mounting lab, expects to learn what customers need as they are taught the intricacies of the technique.

nents Group in Washington, D.C. "There really are no standards, and the rules are being written as the ball game is being played. Already, American manufacturers have pretty much given up the consumer market to Japanese firms, which have settled on some of their own standards. If we don't act soon, we stand to lose large segments in other markets."

Search for security. Meanwhile, components merchants continue their own search for a secure place in surface mounting. Some leading components makers have sought direct connections with surface-mounting trends by purchasing an interest in contract board-assembly houses. Allen-Bradley Co., Milwaukee, has made such a move with AWI of Santa Clara, Calif., while SFE Technologies, San Fernando, Calif., has acquired Orchard Electronics Inc., Concord, N.C.

Taking its lead from the integrated-circuit industry, AVX Corp., Great Neck, N.Y., fashioned its new customer surface-mounting center in Colorado Springs after a similar laboratory that Texas Instruments Inc. opened a year ago in Houston. The facility is housed at AVX's new Integrated Capacitor Division here, and it contains a variety of equipment needed to assemble and test fully loaded surface-mounted boards. AVX lets interested companies use the lab's facilities free of charge.

For several years, North American Philips—with its fingers in both the components and assembly-equipment markets—has been sponsoring three-day seminars at its Surface-Mounted Devices Technology Center in Milwaukee (for more on Philips's SMD activities, see story on p. 38).

"All of the components makers—whether it's resistors, capacitors, trimmers, crystals, or coils—have recognized the situation and see it as an opportunity if not a threat to their established business," notes Jules Hipp, the center's executive director. "We are aggressively suggesting the designers adopt size [of packages] for groups of products worldwide. The purpose is rather obvious but it escapes some people. This [surface mounting] is a manufacturing technology, and key to its success is mechanization, which requires universal standards."

At the month-old AVX Surface-Mount Technology Laboratory, the education efforts are twofold. First, the center provides hands-on experience for potential capacitor customers; at the same time, it aids AVX product engineers in better understanding surface-mounting hurdles.

"The biggest challenge is trying to supply the end user with as much good information as possible," says John Maxwell, marketing manager for advanced decoupling capacitor products and administrator of the AVX laboratory. "Until now, we—the components industry—have not been forced to do that." One result of this is considerable confusion about availability of SMDs, some board assemblers say. Another problem that plagues board makers is a lack of standard sizes for the tapes on which components are supplied for automated assembly.

AVX's surface-mounting work has already resulted in at least one new multilayer ceramic capacitor for the decoupling of random-access memories. The BitGuard capacitor fits underneath standard J-leaded plastic chip carriers, saving up to 10% to 15% of board space (see "Chip capacitor slips under SMD," p. 17).

Understanding. Joe B. Wellington Jr., president of SFE's Orchard contract-assembly subsidiary, notes that there is considerably more to surface-mounting than just doing away with through holes. A thorough understanding of surface-mounted-device technology is critical to successfully converting to the new production technology. "Multilayer ceramic capacitors, for example, are usually the most sensitive element in surface-mounted boards because of thermal shock. If your process will handle them, you are pretty safe with the rest of the parts." Orchard assembles a wide range of SMD pc boards for military, computer, industrial, and telecommunications customers.

INTEGRATED CIRCUITS

IBM GOES TO MARKET WITH SIX VHSIC CHIPS

Las Vegas—Even though IBM Corp. is the world's largest semiconductor producer, the firm has never sold integrated circuits in any quantity to the outside market. Despite this lack of merchant-market experience, however, the firm is among the first of the six prime contractors in phase 1 of the Department of Defense's Very High-Speed Integrated Circuits program to sell chips based on the new technology to outsiders.

At the Government Microcircuit Applications Conference held here in early November, IBM's Federal Systems Division, Manassas, Va., offered catalogs listing six chips for sale to U.S. firms for use in U.S. government contracts. These products included the Signal Processing Element, a 10,000-gate chip offered for use in systolic arrays and other signal-processing applications.

The SPE is based on the same 1.25-μm n-MOS technology that is employed by IBM under VHSIC

Bumps face up in VHSIC-chip package

The VHSIC chips that IBM Corp.'s Federal Systems Division is offering to U.S. government contractors will come in four kinds of packages, among them a novel rectangular ceramic package based on the Decal flexible film module [*Electronics,* Dec. 29, 1981, p. 75). The others are a pin grid array, and, for low lead counts, ceramic dual in-line packages and flatpacks.

Decal was designed by the Federal Systems Division, Oswego, N.Y., particularly for VHSIC chips with a high number of leads—100 or more. In the package, a solder-bumped IC is mounted with the bumps facing up in the bonding cavity of a pinned multilayer ceramic module. Then the bumps are reflowed to chromium-copper-chromium conductors plated onto a thin single-layer-tape polyimide frame. Outer leads on the polyimide are then bonded to pads on the side of the chip cavity.

This technique has several advantages over IBM's usual method of mounting bumped chips face-down to pads on a multilayer ceramic substrate. For one thing, lead lengths in the Decal method are shorter. But more important, the interface between the solder bumps and the tape is more reliable over a wider temperature range (−55°C to +125°C) than the interface between solder bumps and the alumina of the module.

IBM's LSICP (large-scale-integration control processor) is available in a rectangular 240-pin Decal package; several of the other VHSIC-program chips are in rectangular 140-pin Decal-based packages. In each of these package types, the array of pins on 100-mil centers is divided in half by an open ceramic gap; this improves thermal performance because the bare ceramic can contact a cooling element or heat sink.

The Decal method strongly resembles area tape-automated bonding [*ElectronicsWeek,* Sept. 17, 1984, p. 73], which is being considered by Honeywell Inc. for some advanced VHSIC packages. However, area TAB is based on multilayer rather than on single-layer tape. **–Jerry Lyman**

phase 1. The chip has been available for about six months and has already been supplied in small quantities to several firms, says an IBM official. Other chips in the catalog are built using an earlier 2-μm n-MOS process.

One key to the SPE's availability is its status as a much less complex IC than the IBM phase-1 chip on which it is based—the complex multiplier-accumulator chip supplied to the Navy. In fact, the SPE is a simplified version of the CMAC, since it implements only one of the four stages on the 37,000-gate precursor. Yields on the less-complex SPE chip are correspondingly higher, and it will be easier to work with than a full-blown CMAC.

The SPE chip includes a 16-by-16 2's complement multiplier, a 24-bit adder, various pipeline registers, and a control section. The pipelined architecture supports a 20-MHz (typical) operation rate, and multiple chips can be used in an array to improve performance.

Because of the relative costliness of the 1.25-μm-process chips, IBM is not following the usual industry practice of supplying samples at no charge to potential buyers. Instead, the firm is providing samples of the SPE on loan to potential users, says an IBM official. –**Wesley R. Iversen**

SUPERCOMPUTERS

ICOT DETAILS ITS PROGRESS

Tokyo—It was report card time at the International Conference on Fifth Generation Computer Systems 1984, held here this month for Japanese engineers working on their country's Fifth Generation Computer Systems Project. No breakthroughs have occurred in the four and a half months since an earlier conference was held here in late June [*ElectronicsWeek,* July 23, 1984, p. 33].

However, more details were given on work by the Institute for New Generation Computer Technology (ICOT) and on other directly related and independent work in Japan, as well as on work by other groups around the world. ICOT also displayed its personal sequential inference (PSI) machine.

The fifth-generation project is an attempt by Japanese researchers to leapfrog over computer-technology work done elsewhere and into the realm of completely original research. One by-product of this program has been the impetus it has generated for greatly increased efforts into future computational technology in the U.S. and Europe.

Various projects. During a panel discussion on international research activities for new-generation computers, David Brandin, former president of the Association for Computing Machinery in the U.S., outlined a number of projects started by various countries that don't wish to fall behind Japan. In the U.S. alone, projects related to intelligent computer systems include the Defense Advanced Research Projects Agency's strategic computing program, the Defense Department's Very High-Speed Integrated Circuits project, the Microcomputer Center of North Carolina and Semiconductor Research Corp. projects in North Carolina, and the Center for Integrated Systems at Stanford University.

The European Community as a whole has its Esprit program, while the UK is exploring the same area with its Alvey program.

Japanese research continues to benefit from the work in overseas laboratories that has been facilitated by Japan's fifth-generation project. For example, researchers here developing the back-end processors for PSI machines are using a machine language of the type developed by David H.D. Warren of Quintus Computer Systems, Palo Alto, Calif., and Evan Tick, a graduate student at Stanford University and part-time Quintus employee, for a pipelined Prolog processor. Japanese engineers found the machine language to be the best type of language for the job. Warren earlier developed the DEC-10 Prolog language with which ICOT kicked off its research project.

Kazuhiro Fuchi, director of ICOT Research Center, noted that the PSI

Demonstration. ICOT—the Institute for New Generation Computer Technology—had its personal sequential inference machine (PSI) ready to show at the early-November International Conference on Fifth Generation Computer Systems 1984 held in Tokyo.

sequential inference machine and ICOT's Delta relational data-base machine, developed in the initial stage of the project, may be regarded as tools. But they are also more than tools, he noted in his keynote address, because incorporated in them are the basic concepts of the project. Thus, he said they are a reaffirmation of the basic concepts of the project.

Kernel language. The kernel language of PSI is KL0, an expanded version of Prolog used as a machine language. But since it is a machine language, a higher-level programming language called ESP (extended self-contained Prolog) has been developed as a macro-assembly language for KL0. The macro notation provides functional and object-oriented notation.

The operating system for PSI, called Simpos (for sequential inference machine programming and operating system), is completely written in ESP. Simpos is large-scale software (when completed, it will reach about 90,000 lines) and should answer critics who claimed a predicate-logic language could not be used to write control programs such as operating systems.

A look at one direction that ICOT plans to take was given in a paper by ICOT and NEC researchers on "Mandala: A Logic-Based Knowledge Programming System." Mandala is written in KL1, the kernel language that will run on a yet-to-be-built parallel inference machine, and incorporates parallelism in both problem description and execution. It is aimed at developing knowledge-processing systems in a logic-programming framework.

The Mandala language is also a basis for a knowledge-base management system. This dual nature comes directly from the two-sidedness of logic programming; both procedural and declarative interpretation are supported. Moreover, Mandala provides a parallel-execution environment that lets users describe multiple processes. Thus, Mandala supports the ultimate aim of the fifth-generation project of developing a highly parallel computer for knowledge information processing.

Mandala development is still in a very early stage. Its developers have benefited from careful study of other languages, including concurrent Prolog, Loops, KEE, Strobe, Glisp, Krypton, and Smalltalk-80. They have worked closely with Ehud Shapiro of Israel's Weizmann Institute of Science, in Rehovot, and Keith Clark of Imperial College, London, during their extended visits at ICOT. Fumio Mizoguchi of Science University of Tokyo, researchers at other ICOT groups, and still other researchers at NEC, Fujitsu, and Oki are also credited with providing help.

Energizing. In addition to producing the environment needed to obtain funding for projects in other nations, Japan's Fifth Generation project has directly helped to energize the work of some leading researchers in the field. For example, in his paper on "Systolic Programming: A Paradigm of Parallel Processing," Shapiro thanked ICOT researchers for the stimulating environment they provided while he worked there.

Shapiro advocates a systolic programming approach that is potentially applicable to general-purpose multitasking, multiuser computers. He says that arbitrarily large approximations to the infinite abstract machine are realizable using current technology, and that unless a parallel processing method is infinitely scalable, the parallel-processing problem will have to be re-solved every two years when the number of processors doubles. **–Charles L. Cohen**

TESTING

DOUBLE-THREAT MACHINE CUTS RAD-HARD-TEST COSTS

Las Vegas—Testing for radiation hardness in military integrated circuits has traditionally been a time-consuming and costly affair. In order to get the proper irradiation sources to do the required testing, military chip makers usually have been forced to send expensive test personnel and equipment to an off-company facility that offers use of a linear accelerator, for example, or a Cobalt-60 irradiation source.

What's more, the use of such facilities requires that parts be fully packaged for testing. This means that if sample parts tested don't meet a program's specified radiation-hardness requirements, then the entire production lot must be rejected.

Pair of sources. Now a small Sunnyvale, Calif., firm known as Advanced Research and Applications Corp. (Aracor) says it has a solution to these problems. Using technology adapted from government contract work at Aracor and elsewhere, the

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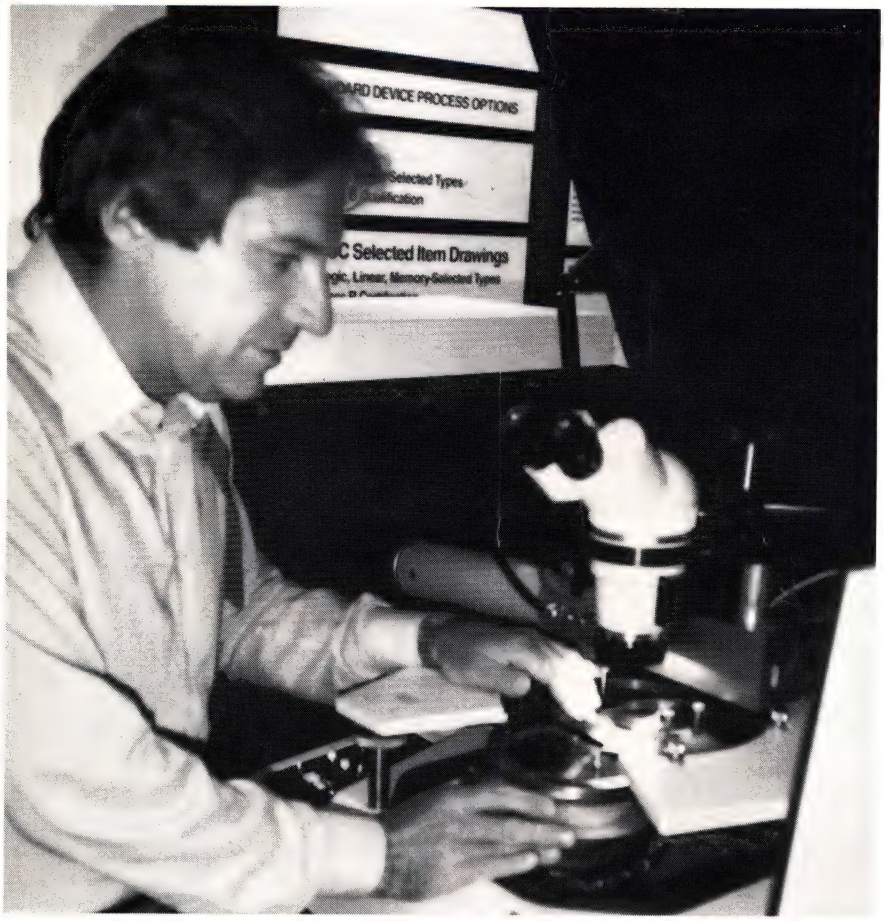

Doubled up. Aracor's tester has two sources of irradiation: a 10-KeV tungsten X-ray source for exposing chips to heavy doses, and a Nd:YAG laser to induce electrical transients.

firm has built a machine designed for use on the IC production floor that integrates two types of irradiation sources into a cabinet measuring 33 in. wide by 72 in. long. Not only can the unit obviate the travel requirements for some types of radiation testing, but it also allows screening to be done at the wafer level instead of at the level of fully packaged parts, points out L.J. Palkuti, manager of Aracor's Semiconductor Technology Department.

Palkuti gave a paper on the system earlier this month at the Government Microcircuit Applications Conference here, and Aracor was pushing the unit for sale on the Gomac exhibition floor. Known as the Model 4100 Automatic Semiconductor Irradiation System, it incorporates both a 10-keV tungsten X-ray source and a 1.06-μm neodymium-yttrium-aluminum-garnet (Nd:YAG) laser. Aracor was able to tuck both sources into the 4100 largely because of its compact power supply for the X ray and a folded-beam design for the laser.

By collimating the X-ray beam, irradiation doses can be directed at a specific die at dose rates ranging from 50 rad/min (SiO_2) to 150 Krad/min (SiO_2) to provide the kind of total-dose testing usually done at an external Cobalt-60 source site. A die can be be exposed in about 7 minutes to 1 megarad (SiO_2), which is a typical military goal for radiation hardness, Palkuti explains. Measurements have revealed that adjacent dice receive only 0.1% of the exposure of the specific die being irradiated in a test, Palkuti adds.

The Nd:YAG laser source, by contrast, can be used for testing a circuit's ability to withstand radiation-induced transients, a type of testing that has conventionally been done at remote sites equipped with linear accelerators or large flash X-ray units. Based on a pulse-width range of 15 to 100 ns at 10 pulses/s using the 350-mJ laser, dose rates as high as 2×10^{12} rad/s (Si) can be obtained, a level sufficient for current test requirements.

Test time slashed. At Hughes Aircraft Co.'s Industrial Electronics Group Technology Center in Carlsbad, Calif., senior staff physicist Kenneth G. Aubuchon says that the firm has been using an X-ray-only Aracor machine for about 18 months. It has enabled Hughes to reduce the time required to do total-dose testing from more than a week to a matter of minutes, since the firm is no longer required to package samples and travel to a remote testing site.

Because the 4100 appeals primarily to military chip contractors, Aracor estimates that the total market for the system could amount to about 20 units, says S. Thomas Workman, the firm's vice president. Others have speculated that demand may be higher, however, perhaps for as many as 200 systems. A 4100 equipped with only the X-ray source sells for about $155,000, and a version with both types of irradiation sources carries a price tag of about $255,000. **–Wesley R. Iversen**

SOFTWARE

FRENCH INDUSTRIAL QUARTET TAKES FLING AT SOFTWARE

Paris—About to take a foray into the software business are four large French organizations that normally make their respective livings outside the electronic data-processing business. What they will be peddling is nothing less than a jointly developed program that they are touting as the first global optimization program for energy costs.

The collaborators are Serete SA, one of the country's largest engineering firms; Société Nationale ELF Aquitaine, the country's principal pro-

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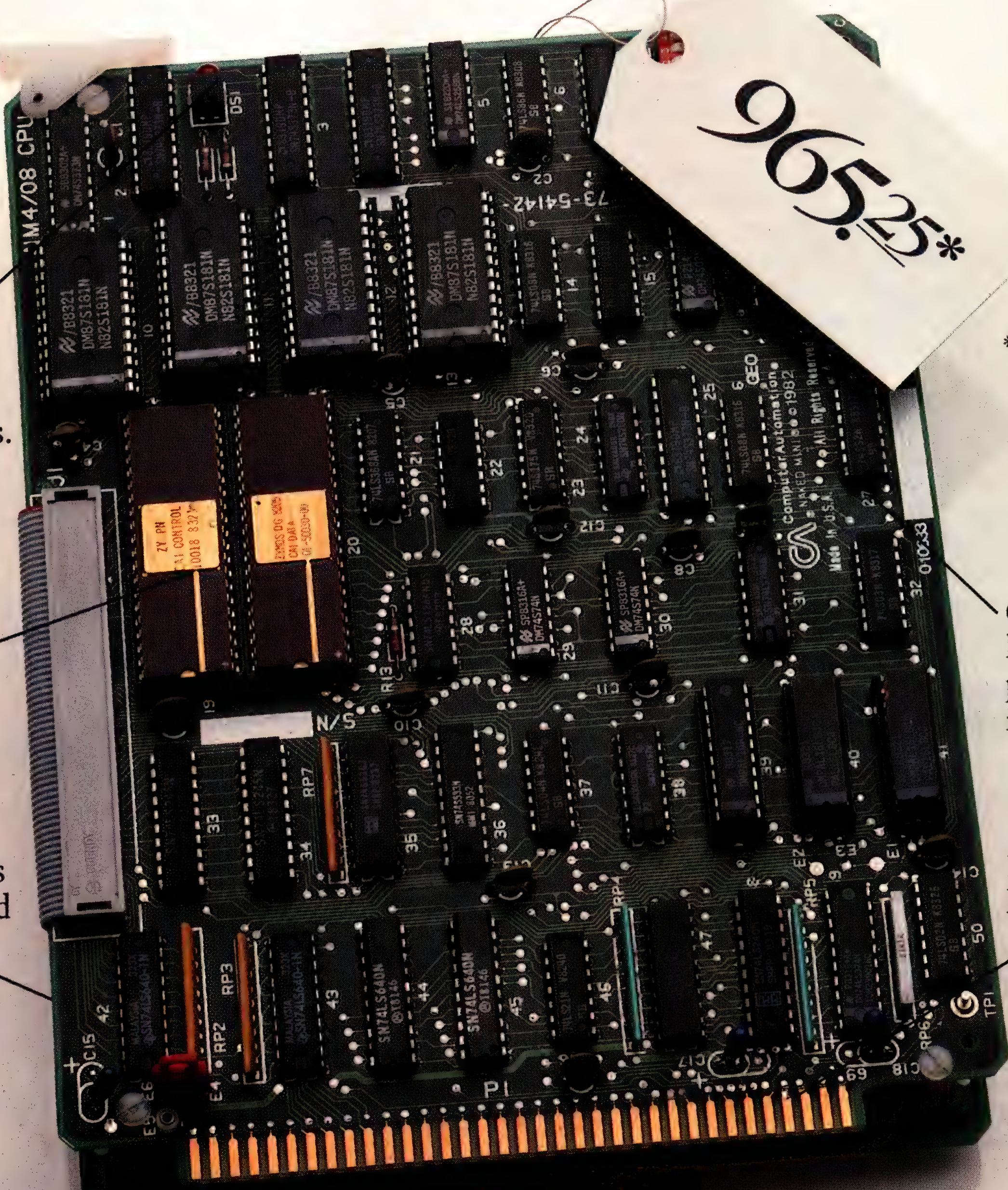

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Not bad for software tyros

Even if the four organizations that developed SECI Manager—two construction companies, an oil company, and a research institute—do not do data processing for a living, their product is an impressive piece of software development, both architecturally and functionally.

Consisting of some 30,000 instructions written in Fortran, SECI Manager can be run in modular fashion on computers with as little as 64-K bytes of available memory, though on larger machines it is executed in modules of some 300-K bytes.

The heart of the program is a central modeling unit that interfaces with the program's other modules to carry out simulation, optimization, and coherent measurement adjustment. Basically, the central module transcribes, in mathematical form, the reality of a site. It includes a standard library of equipment normally encountered in energy configurations such as boilers, gas or steam turbines, pumps, condensers, process machinery, and so forth. A schematic description of the actual site is executed simply by connecting different pieces of equipment from the library.

In one of the trials of SECI Manager carried out by the four organizations, a complex industrial site that included a maximum of different kinds of equipment was modeled. Simulation of the site then required only several seconds of time on a mainframe computer and produced results that the four developers of the program term "surprising."

In analyzing the marginal costs of producing steam, for example, they noticed differences of as much as 20%, depending on which of the system's boilers was servicing marginal demand at a given time. SECI Manager was able to optimize these differences systematically by taking into account such factors as the relevant bracket of utility rates, the respective loads of the boilers, and the recovery of calories. –R.T.G.

---

ducer of oil and petroleum products; Cosmip Entreprise SA, a subsidiary of the Compagnie Générale d'Electricité, which specializes in industrial automation and electronics; and the Institut Français du Petrole, a government-supported agency devoted to petroleum-related research and development.

The partners assert that their program, called SECI (for their respective initials) Manager, can handle energy management for any industrial site regardless of its size or complexity (see "Not bad for software tyros," above). Existing energy-management programs, they say, treat energy optimization only for isolated pieces of equipment or for certain limited equipment configurations.

Filling a vacuum. Their plan is to fill this vacuum with an easy-to-use program based on user dialog, which, in its first generation, can take as inputs characteristic values of industrial energy systems such as fluctuations in fuel flow, power, total heat (enthalpy), system regulation apparatus, condition and yield of equipment, and even utility rates for all existing energy supplies.

SECI Manager, which requires no expertise in data processing, then uses this data to put out operational simulations of the model thus constructed, as well as optimization models. The optimization models indicate how to achieve the minimum operational cost for a system, while taking into account the limits and constraints imposed by the user.

A future version, which the four say will be available next year, will operate in real time. It will take inputs from on-line sensors, as well as the operator, to directly manage a given energy-consumption system under optimal conditions.

The program's efficiency, say its creators, is largely the result of its being based on algorithms derived from real energy-consumption and -utilization curves. Other energy management programs, they claim, are based on linear calculations.

Coherent. In addition, the real-time version will incorporate a coherence module that corrects data from sensors as a function of the known precision of the sensor and related measures from other sensors. The result is a product that straddles the line between a computer-run management program and an expert system.

The four groups are convinced that their invention is the most cost-effective way of dealing with an almost impossibly confused problem. "When you take into account the complexity of industrial sites as well as the continual change of the global energy landscape, it makes it extremely difficult to find the right strategy to optimize energy consumption," explains Gérard Sarrazin, deputy director of ELF Aquitaine's Energy Economics department. But even a limited saving would in most cases justify the cost of the program, he reasons. **–Robert T. Gallagher**

DISPLAYS

TOUCH-INPUT FIRM MOVES TO TOUCH NEW MARKETS

Austin, Texas—Officials at Carroll Touch, AMP Inc.'s touch-technology subsidiary here, believes the company has a finger on what it will take to turn touch input into a high-volume business: lower cost. Intending to shatter what may be a cost barrier blocking greater use of scanning-infrared touch technology, the firm will announce this week an integrated screen-input subsystem that halves the price of such products.

The AMP unit's approach to scanning-IR touch entry has been re-engineered to incorporate a Motorola 68705 single-chip microcomputer. The 8-bit microcomputer has 112 bytes of random-access memory, 4-K bytes of read-only memory, and a 4-channel converter. Among other things, it allowed Carroll Touch to improve the screen's immunity to

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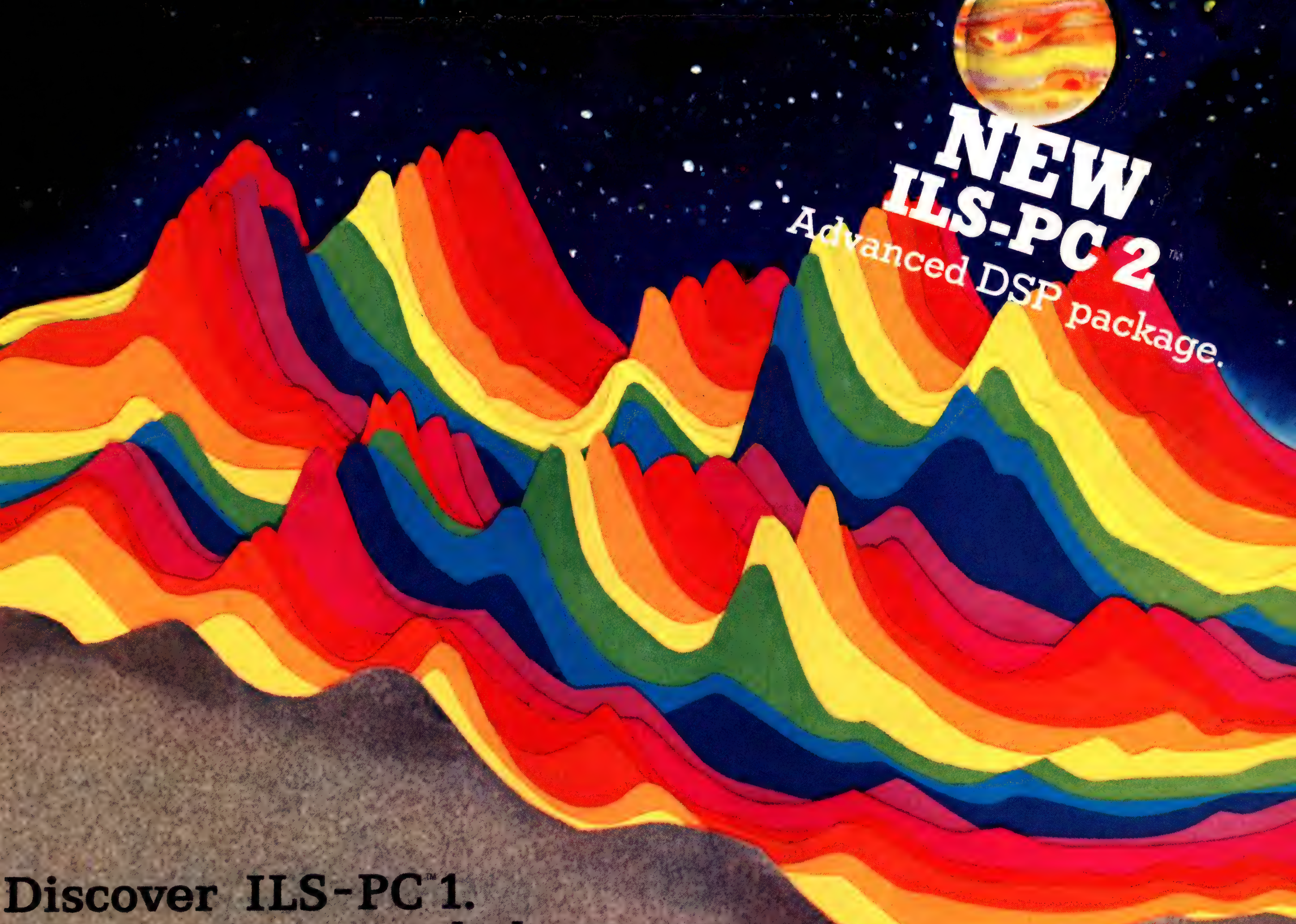

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ambient light by a factor of four.

Compared to its existing IR touch-sensing systems, the 8-bit chip and new on-board firmware cut the number of devices by 45%, says Arthur B. Carroll, founder and chief executive officer of the operation, who sold a majority interest to AMP last year. The new Smart-Frame series integrates all the electronics needed for touch-entry onto the optoelectronics frame that is placed around the front of the display screen.

Deft touch. Arthur Carroll thinks the use of infrared touch screens will explode into consumer applications now that prices are down.

That reduction, plus an aggressive manufacturing ramp-up at its plant in Champaign, Ill., has let the firm cut the price to $595 from $1,180 for touch-sensitive systems on 13-in. cathode-ray-tube screens; 19-in. CRT systems are being reduced to $795 from $1,415 in single quantities. For large quantities, the new 9-in. Smart-Frame could cost as little as $150.

Low plateau. "We want to break that chicken-and-egg game by saying, 'Here is IR touch at an affordable price.' We think the only reason that kept it out of many high-volume systems was that the price has pushed us out of the cost window," says Carroll. "With this new product, we think we have established a new plateau, and we intend to further lower that level."

At the new price, AMP believes the technology will finally appear in high-volume products: cars, consumer systems, industrial automation, and process control. International Resource Development Inc., a Norwalk, Conn., research firm, sees touch-input-system sales jumping from $15 million in 1984 to $116 million in 1988.–**J. Robert Lineback**

DESKTOP PROCESSOR USES CARTRIDGES

Watford, England—One British maker of data-communications gear is updating the time-honored game of "kill the competition" by using a video-game trick to play it. The company, Computer and Systems Engineering plc, or CASE, has come up with a desktop communications processor that is several products rolled into one. By simply exchanging a cartridge module, similar to a video-game cartridge, the 81X Openline becomes, in turn, a point-to-point or switching multiplexer, an X.25 packet-assembler and disassembler, or a protocol converter.

"This cartridge is the Micom-killer, and this one is called Goodbye Timeplex," says CASE sales and marketing director Michael Hafferty as he hefts two small black boxes. His somewhat flippant remark refers to Micom Systems Inc., Chatsworth, Calif., which pioneered the market for low-cost, over-the-counter statistical multiplexers, and to Timeplex Inc., Woodcliff Lake, N.J., a big player in the market for dual-link multiplexers.

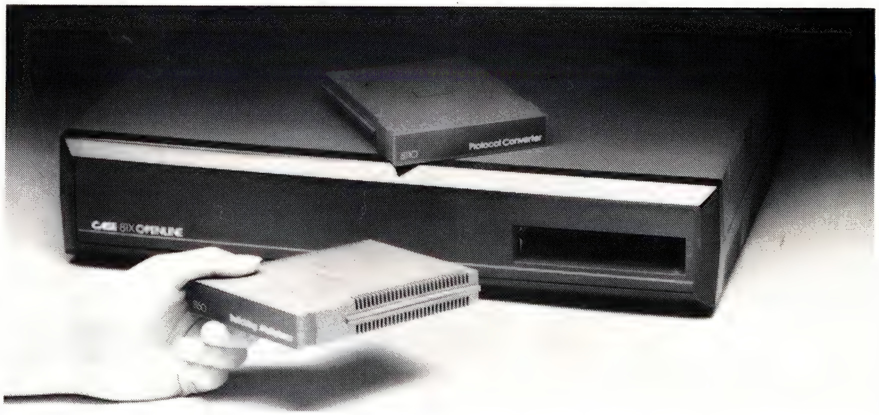
For all his tongue-in-cheek salesmanship, Hafferty's remark does carry one clear message: CASE intends to lock horns with its many U.S. competitors. Until now, the fast-growing Hertfordshire company has focused on the market for large data-communications networks, blazing a trail with its DCX exchange, which it launched in 1979.

The 81X Openline, shown for the first time at last week's Comdex show in Las Vegas, takes CASE into new territory. With Openline, the company believes it can participate in three separate markets and create a new one.

Polarized market. The statistical multiplexer market has polarized, says Hafferty. At one end, several companies are scraping along with cheap, point-to-point-wired models. At the other end, heavyweight equipment manufacturers are offering fancy switching multiplexers largely modeled on the DCX.

Openline occupies the middle ground for small, low-cost data networks, Hafferty claims. In general, he says, a small network would cost between one half and one quarter the price of a network with the same number of nodes, built with current top-end products.

The system's ability to change functions by plugging in a different read-only-memory cartridge provides users with a flexibility that can protect their investment. One bank, for example, is ordering the 81X as a multiplexer, but wants to change to a



Pop goes the program. The entire functionality of the CASE 81X Openline desktop communications processor can be changed by inserting a new Program Option Package—similar to a video-game cartridge—into the front panel.

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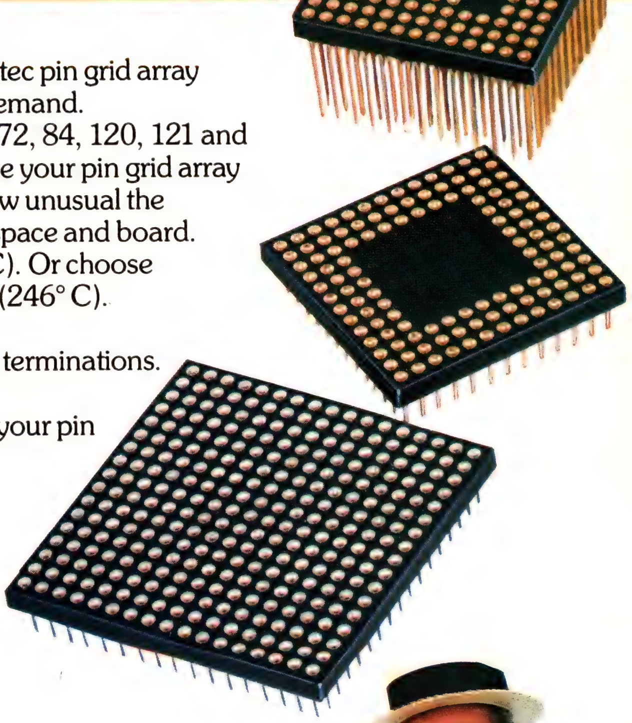

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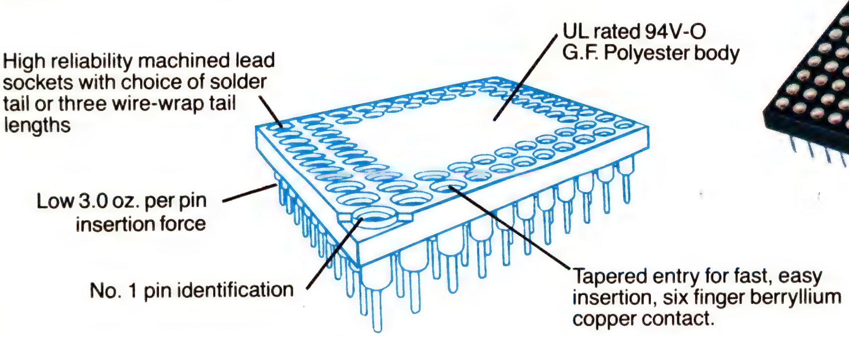
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packet-switched network later. “All you have to do is pop in a new cartridge and away you go,” he says.

Each cartridge contains the entire control program for the single-board Motorola 68000-based communications processor. The cartridges, priced between $720 and $1,740, are called Program Option Packages, or POP-PACs. Complete systems range in price from $1,440 to $3,000.

Works with dummies. The first two products are five- and nine-port statistical multiplexers. Each can be used to combine a number of asynchronous dumb terminals into a single synchronous composite link running at 19,200 b/s. Typical channel speeds are from 50 b/s to 9,600 b/s. A single printer can be shared among terminals, a handy feature in sales or reservation systems. Different types of terminals are handled by built-in emulation.

Up to nine sites and 72 terminals can be strung together into a network by using several of CASE's 8140s. Thanks to their dual-channel capability, local- or wide-area networks are easily formed by daisy-chaining several multiplexers together. Any terminal can be used to configure the network. Multiplexers in the network will then perform speed- and flow-control conversion between other incompatible components.

The 8150 can be networked in the same way but also lets users dial up data ports anywhere in the network. This flexibility means that the terminals can be used to transfer documents and files anywhere in the network. Without knowing anything about the network, says Hafferty, a user could call up a Digital Equipment Corp. VAX and be routed through. If the port is busy, he can queue or just ring back.

The 8160 gives cheap access for up to eight asynchronous terminals to the packet-switched network, or it can be connected to a mainframe. As with the 8150, addressing is easy—the terminal will translate an easy-to-remember mnemonic into the needed 14-digit address.

CASE expects to offer many protocol-converter products and is kicking off with an 8110 converter. This connects asynchronous terminals into the IBM Corp. bisynchronous network by emulating an IBM 3274 cluster controller. Up to eight terminals are supported at speeds up to 9,600 b/s.

With its multifunction product, CASE can address several high-growth markets. The worldwide market for multiplexers of comparable capacity already stands at $260 million this year, it says, and is projected to rise to $800 million by 1988, over half of it in the U.S. The packet-assembler-and-disassembler market, too, is growing at 55% a year, and it should be worth some $150 million by 1988. The market for protocol converters, meanwhile, is growing at around 30% annually. With this and growth from new applications, CASE says it is targeting a market worth $1 billion by 1988.

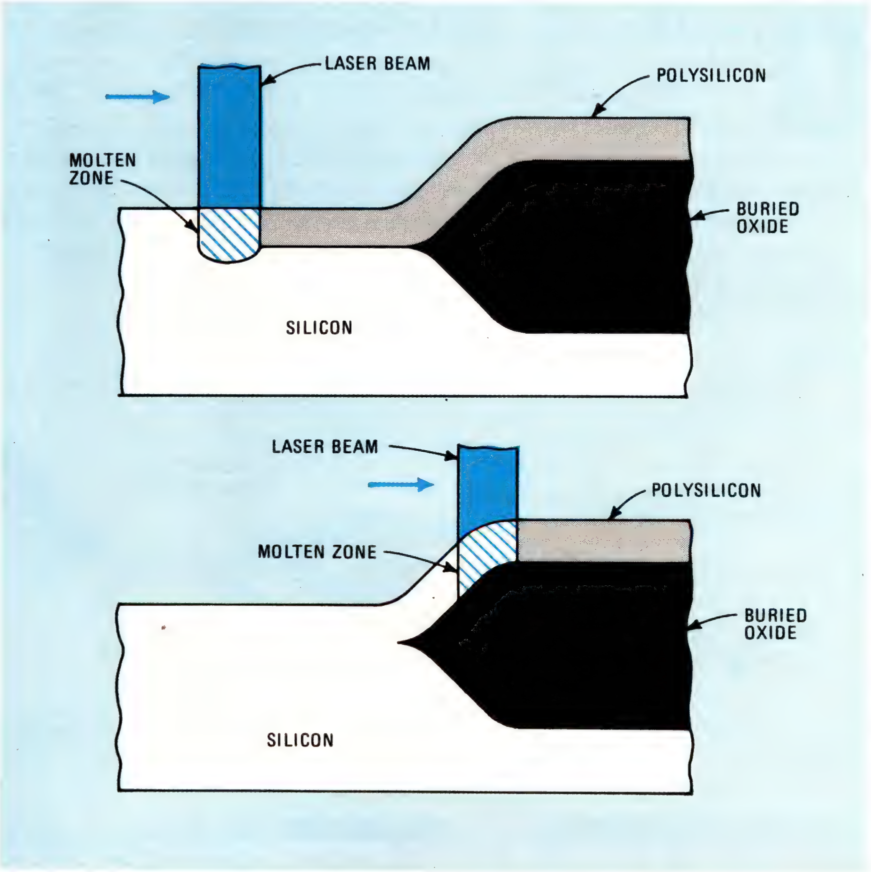
–**Kevin Smith**

SEMICONDUCTORS

SOI METHOD CAN BE USED IN SUBMICROMETER ICs

Grenoble, France—In a development that could well augur the coming of age of silicon-on-insulator technologies, a team of French engineers has developed a seeding technique that permits the uniform recrystallization of polysilicon films on oxide layers. Adding significantly to the appeal of the method, the resulting substrates can serve as the basis for fabrication of micrometer- and submicrometer-scale devices for integrated circuits using standard design rules and a nearly standard process.

Developed at the Laboratoire d'Électronique et de Technologie de l'In-



Going to seed. By beginning recrystallization of a polysilicon layer where it is in contact with a bulk silicon substrate, LETI takes advantage of a seeding effect that uniformly crystallizes the material atop a layer of silicon dioxide. The nitride layer on the polysilicon aids heat distribution.

formatique (LETI) here, the method has already been used to produce a number of test circuits. The results outstrip any SOI figures heretofore published [*ElectronicsWeek,* Aug. 6, 1984, p. 31], according to LETI's director of microelectronic research, Jean-Pierre Lazzari.

What's more, in terms of leakage current—perhaps the most significant parameter in determining the electrical quality of SOI transistors—LETI's process realizes devices showing a fivefold improvement over the best of the notoriously expensive silicon-on-sapphire technologies.

Standard beginnings. LETI's process begins with a standard silicon substrate upon which 2,000-Å-thick stripes of silicon dioxide are deposited about 10 μm apart. The spaces between the oxide stripes serve as windows to provide substrate access. A layer of polysilicon, also 2,000-Å thick, is then deposited on the entire surface, followed by a thin nitride capping layer.

Recrystallization of the polysilicon is achieved using laser annealing. Initially, a laser beam is focused on the polysilicon deposited on one of the windows in the oxide. When this material becomes molten, it tends to react with the Si substrate with which it is in contact to become a seeding layer, in much the same way that the structure of a pyramid consisting completely of spheres is determined by the base layer. As the laser spot scans away from the window toward the SiO_2, the polysilicon that is deposited on it follows an identical seeding pattern.

Thanks to this seeding effect—as well as to the nitride capping layer, which ensures uniformity of temperature beneath its surface—the method yields stripes of monocrystal silicon the length of the wafer and with a width of from 20 μm to 50 μm. This is easily large enough for the fabrication of MOS transistors.

From that point on, IC production is standard, with the exception of implantation processes that must be adapted to the thin-crystal film, which replaces the substrate bulk in standard processes. Circuit designs must be configured so that only the circuit's nonactive sectors, such as interconnections, reside on the areas that served as windows. According to Lazzari, this poses little difficulty.

Using substrates thus prepared, LETI has produced a 101-stage ring oscillator that exhibits a propagation delay of 93 ps at a supply voltage of 5 V—a velocity gain of more than 40%, compared with the same oscillator produced in a standard bulk process.

Though the laser-recrystallization step could pose production problems, LETI researchers say they are closing in on an answer to that, too. The laboratory is developing a completely automated recrystallization machine, which it expects to exhibit a throughput of between 60 and 100 wafers per hour. –**Robert T. Gallagher**

FOREIGN TRADE

JAPANESE TO ENACT EXCLUSIONARY TELECOM LAW

Tokyo—The next major U.S.-Japan trade conflict can be summed up in a single word: telecommunications.

The Japanese telecommunications market, valued at $4 billion last year and expected to exceed $8 billion by 1987, is supposed to become more open to foreign participation when reform legislation takes effect next April. But another barrier has been erected, in violation of normal Japanese administrative practices.

A study of the issue, commissioned by the U.S. Embassy in Tokyo and circulated to trade officials in Washington, charges that despite assurances from Japanese government officials, an exclusionary telecommunications equipment standards and certifications system is being set up. According to one U.S. official, the system "takes us back to the feudal era, when foreigners were banned from Japan."

Under the draft Telecommunications Enterprise Act of Japan, a Designated Approval Agency is to be formed to serve as the sole testing and certification body for telecommunications interconnection equipment to be used in Japan. But instead of the impartial group described by the Ministry of Posts and Telecommunications (MPT) in meetings with U.S. officials several months ago, an agency has been formed that is completely closed to participation by U.S. industry.

Movers and shakers. Moreover, the dominant players include major Japanese telecommunications makers, as well as the Nippon Telegraph & Telephone Public Corp., which is supplying the laboratory site and technical staff. To top it off, the entire project has been financed by major Japanese banks.

Normal governmental procedures such as informing Cabinet offices were avoided. The project's secrecy was so complete that many NTT officials, who themselves support a freer, more competitive market, did not know of the association until they saw the U.S. Embassy report.

The association, which came into formal existence in late October, cannot be authorized until two new telecommunications laws—one privatizing NTT, the other setting more liberal standards for participation in so-called value-added-networks—are passed by the Japanese Diet next month. But that is expected to be a formality.

The new group's authority would include the sole right to inspect telecommunications terminal equipment, issue labels of product approval, and control the dissemination of technical standards. It would also provide influential comment on the setting of MPT telecommunications equipment technical standards.

Mark Foster, an attorney in Tokyo who advises the U.S. Embassy on technical standards and procedures, describes the Japanese action vividly: "Imagine IBM, Burroughs, Texas Instruments, and Wang going to the FCC and asking for approval to set up an exclusive organization to certify all telecommunications equipment in the U.S. market, with financing from Morgan Guaranty and Bank of America."

Isao Asamura, the director of the

new agency, has said publicly that the group does not intend to accept U.S.-generated technical data. Moreover, he says, inspection applications must be written in Japanese.

Japanese officials have tried to blunt criticism of the exclusionary nature of the agency by noting that it includes such foreign-based Communications Industry Association of Japan (CIAJ) members as Motorola Inc. and Northern Telecom Ltd. "But that doesn't help all the little guys," argues John P. Stern, a representative of the American Electronics Association-Japan. "We have an estimated 2,700 members, and most of them are small firms with no Japan office. How are they going to compete in this atmosphere?"

Faced with what amounts to a *fait accompli*, the U.S. side has little time to act. A U.S. government trade team was in Tokyo last week for talks that included the standards and certifications issue, but an American industry source admitted, "We're still not unified on this."

Jack McDonnell, vice president of information and telecommunications technologies for the Electronic Industries Association, was in Japan recently to question Japanese officials about the legislation. "We have a window of between 60 to 90 days to affect this legislation and the way it is implemented," he says.

Public clamor. One approach would be for U.S. firms to raise the sort of public clamor the computer makers did earlier this year in opposing Japan's controversial software-protection proposal. But even so, as one electronics executive put it, "If we got all the changes we wanted, how much could U.S. companies sell in Japan?"

A partial answer to that question comes from securities analyst Bernard Key of Jardine Fleming Investment Services Ltd.'s Tokyo branch: "The major Japanese telecommunications makers have been in the marketplace for months, getting orders from their usual customers and making future arrangements for supply and delivery. Any foreign firm with a serious idea of getting into this market should have begun its work three years ago, when those first fiber-optic cables started going into the ground."

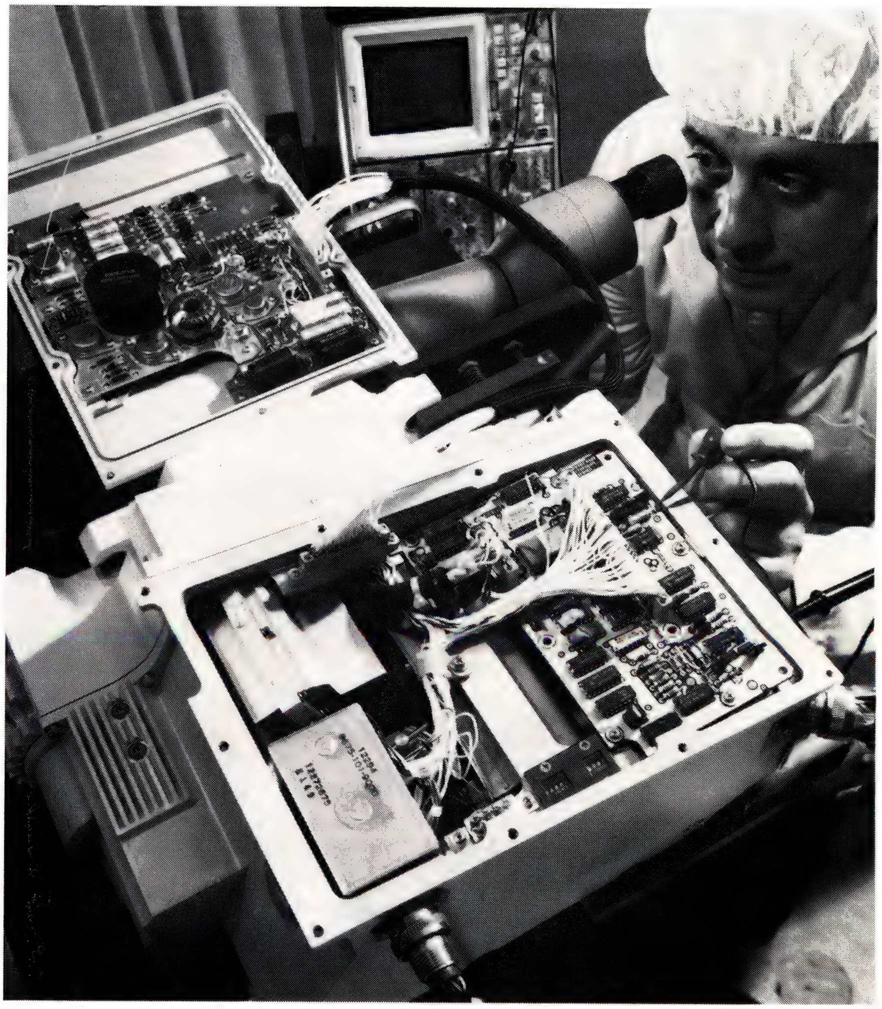
–Mike Berger
McGraw-Hill World News

CO_2 LASER RANGE FINDER WORKS IN PROTOTYPE

El Segundo, Calif.—One rap against high-technology military gear is that it needs nearly perfect conditions to do the job. The U.S. Army's solid-state laser range finders, for example, work fine in spotting tactical targets when they're clearly visible, but they cannot cope with the smoke, haze, and dust that typically obscure a battlefield. Because improving tactical range finding ranks as a top Army priority, Hughes Aircraft Co.'s development of the first carbon dioxide laser for this application is an important milestone—albeit an early one.

Hughes's Electro-Optical and Data Systems Group here has been at work on the CO_2 laser for nearly five years, but only since 1982 have some of the necessary components been available. "The limitation all along was the laser transmitter," explains Richard Salotti, program manager. At the time, its size prevented a working laser from fitting into the internal mounting envelope inside the M1 Abrams battle tank. Also, power levels were inadequate, and the only sources for laser transmitters were foreign firms, not permitted in military procurement.

Accordingly, Hughes launched its



Shedding new light. Army field tests have shown that this CO_2 laser range finder is better able to penetrate smoke and dust than current solid-state lasers.

own program to upgrade the transmitter's power by a factor of three to four, while reducing its size. Though Salotti is not divulging any specifics about the transmitter's performance, the program has been successful enough for a prototype model to be delivered to the Army for field tests. Eventually, the Army intends to use the CO_2 laser to replace neodymium-yttrium-aluminum-garnet units, also supplied by Hughes, which have been in service since the late 1970s.

Compatibility. In operation, a tank gunner aims the range finder at a target, from which the laser beam reflects back into a receiving telescope. The range is determined from the elapsed time of laser-beam travel—data that feeds into the fire-control computer. The main advantage offered by a CO_2 laser is that it works on the same wavelength, 10.6 µm, as the thermal-imaging system that the tank's gunner uses to spot targets.

By contrast, the YAG range finder operates at 1.06 µm. "A CO_2 laser gives the gunner the ability to determine the range of any target he can see with the thermal imager," notes Salotti. Hughes reports that when it was tested with the M1 tank's primary sight, the range finder ranged on all targets that could be picked up by the imager at distances from 200 to 8,000 m.

The CO_2 laser works as well as the YAG unit under optimum conditions, but heavy rain or fog impairs its thermal imaging. On the other hand, a big advantage that the CO_2 laser has over the YAG is that it is harmless to the human eye. "This is unimportant in battle," says Salotti, "but it makes a difference during training exercises."

Hughes developed the CO_2 range finder under a contract with the Army's Night Vision and Electro-Optics Laboratory. Evaluation of the unit is continuing. **–Larry Waller**

SEMICONDUCTOR PROCESSING

POLYMER PHOTORESIST DEVELOPS ITSELF

Albuquerque, N.M.—Among the items on semiconductor manufacturers' wish lists, self-developing photoresists rank near the top. Their attraction, of course, stems from doing away with the complex—and expensive—processing required to create an image on each layer of an integrated circuit.

Industry researchers therefore are fast picking up on the discovery at Sandia National Laboratories of a new class of silicon-based polymer materials, a discovery that could lead to self-developing photoresists. The new material is a polysilane copolymer, made from an inexpensive chemical used in rubber production.

The advantage of polysilanes is that when subjected to deep ultraviolet light, at a 2,500-Å wavelength, they break down into smaller molecules that vaporize as nontoxic waste gases. "Where the UV light hits, in other words, the material disappears," explains John M. Ziegler, Sandia organic chemist and co-discoverer of the polysilanes. Physical chemist Larry A. Harrah was the other principal scientist on the project.

UV-sensitive. The scientists quickly realized that the material, when applied as a film on a silicon wafer, could be self-developing when exposed to UV light projected for about one second in a circuit pattern. Tests at Sandia confirm this potential, Ziegler says, along with demonstrating the extraordinary sensitivity of the material to UV light. It is from 20 to 60 times more sensitive for removing material than are commercial materials and conventional solvents, the tests show.

This quality itself opens up another advantage for the new material for use with new generations of ICs: high resolution of the resulting circuit patterns. Features as small as 0.8 µm have been achieved in the laboratory, and "that is not the best

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we can do," observes Ziegler.

Furthermore, the polysilanes are sensitive only to UV light, which means that darkroom precautions are not necessary to protect them from degrading in visible light. Physical properties also are promising for IC production; thermal stability is higher than present resists, remaining intact up to at least 350°C. In addition, it is strong and will adhere well to quartz, silicon, and aluminum, according to Sandia.

Firm inquiries. While several processing-equipment firms already have approached Sandia for more data on the material, Ziegler notes that more work must be done before it becomes a commercially sound technique. For one thing, how it relates to dry-processing techniques that employ plasmas to etch circuits must be further investigated, specifically with freon gas. It is already proven with bilayer lithography.

One problem the photo-patternable polysilane avoids is toxicity, which has plagued other self-developing approaches. "It does not give off materials that are toxic or corrosive," Ziegler says. "It is not even a skin irritant."

As for the impact on ICs, the opinion of process consultant Will Strauss, vice president of In-Stat Inc., Scottsdale, Ariz., is that the Sandia discovery seems "worth the time, effort, and money necessary to see if it works. The key points are exposure time and sensitivity, since these directly influence throughput," he says.

Redesign questions. Other considerations are how much redesign of equipment would be called for. An example is applying the material onto wafers; polysilane has a higher viscosity than present photoresists, ruling out a spin technique.

Ziegler believes that first commercial applications are several years away, initially on simple ICs. The timetable could change, however, as interest picks up. Researchers at IBM Corp.'s laboratories in San Jose, Calif., for instance, have been investigating nearly similar materials, but without self-developing characteristics. However, they have changed directions recently, Ziegler says, to more closely track the findings at Sandia, which is operated by AT&T Technologies. –**Larry Waller**

AI SYSTEMS

UK ACCENTS VOICE GEAR

London—The British government has thrown its weight behind a handful of high-technology firms in an effort to capture the world lead in voice-controlled equipment. Along with a voice-operated word processor for the Alvey directorate's fifth-generation computer project [*ElectronicsWeek*, July 23, 1984, p. 52], the effort is focused on:

- Voice-controlled navigation and radio gear for future fighter aircraft, backed by the Ministry of Defence.
- Rugged low-bandwidth, voice-operated communications links for use in civil aviation, military, police, and other operations, also backed by the Ministry of Defence.
- Telephone inquiry services that team speech recognition and synthesis with knowledge-base expert systems, also an Alvey project.

For the Alvey word processor, whose goal is a 5,000-word vocabulary and the ability to handle conversational speech, group leader Plessey Co. plc will have to develop blue-sky technology. But for the trio of new projects, less adventurous technology will be put to work.

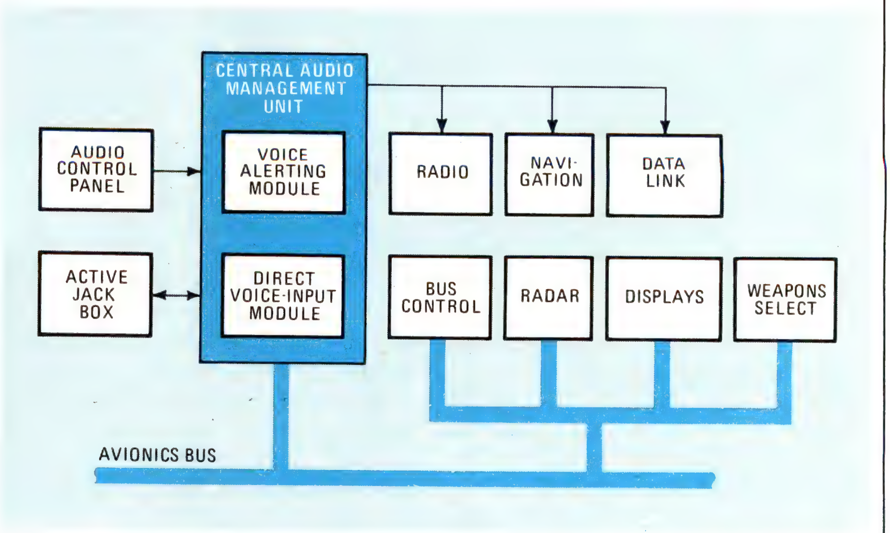
To move quickly into production, off-the-shelf equipment from Marconi Secure Radio Systems, Portsmouth, and Logica plc, Cambridge, will be used. Marconi's SR-128 and Logica's Logos kit both make use of advanced research in electronic intelligence gathering at the government's Joint Speech Research Unit, Cheltenham (see "Matching words rather than phonemes," p. 37).

So far, both systems can recognize the rudiments of conversational speech, and they do not require a speaker to pause between words—still a rare feature in voice-recognition gear. Both systems work by matching stored-word templates with incoming speech.

The basic difference between the two is that Logos was developed as a general-purpose research tool and has modular microprocessor architecture, while SR-128 was developed as a dedicated voice controller. It could, for example, be used for data entry, inspection, baggage handling, and computer-aided design, and on the flight deck.

Off the ground. A government research aircraft has in fact been flying for over two years with Marconi's speech-recognition equipment on board. It has been used to control moving-map displays as well as navigation and radio gear. Now, the Ministry of Defence is going to request proposals for a production system. One possible candidate for the gear is an advanced fly-by-wire fighter now being considered as a joint European venture.

Because Marconi developed the Royal Aircraft Establishment Bed-



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experimental voice controller, it stands a good chance of winning the UK contract. But Racal Electronics plc and Smiths Industries, Aerospace and Defence Systems Ltd. have licensed Logica's Logos technology, announced at September's Farnborough air show, and are also likely to submit bids.

Voice control will first be applied to the aircraft's navigation and radio gear. The equipment could be designed to act on instructions such as "Select radio frequency 125.250" or "Select IFF code 1234."

"The pilot does not have to remember the frequencies," explains Jeff Wilson, division manager of speech systems at Marconi. "He could say 'Bedford Tower' and have the speech recognizer pass this information to the flight computer."

The voice-control system could also be used as a communications link in military, police, and other operations where routine messages make up a lot of traffic. A possibility is low-bandwidth ground-to-air satellite communications. Racal, for one, is flight-testing such a link for navigational data. With a data rate of 50 b/s, it could be modified to carry encoded voice messages.

Keeping time. Back on earth, Logica's Logos technology is at the center of a soon-to-be-announced Alvey project to demonstrate an automatic train-timetable service that can be accessed by telephone. The three-year, $2.4 million project unites British Telecom plc as project leader, Logica's Cambridge research center, and Cambridge University.

Because the service will be used by the public, Logica's recognition gear must be speaker-independent—like most systems, it must currently be trained to recognize a new speaker. But Logos's project leader, Jeremy Peckham, says that template-matching technology still has a lot of stretch. One considerable advantage is that it takes only a limited vocabulary to handle train inquiries.

Even so, an expert knowledge-base approach will be needed. And one has been developed by Stephen Young at Cambridge University. It analyzes questions for their meaning and answers them.

It also aids the template-matching recognizer by adjusting the recognizer's active vocabulary to the context. When the time is being asked, for example, number templates are loaded into the vocabulary. A voice synthesizer, developed by Frank Fallside at Cambridge, will give callers the train times.

The project has been under way for several years at British Telecom and is being widened with Alvey funds to produce a full demonstrator system. Telecom will work as project coordinator; its human-factors group will evaluate the system's acceptability. –**Kevin Smith**

Matching words rather than phonemes

The connected-speech recognizers that have been developed separately by Marconi Secure Radio Systems and Logica plc draw on advanced speech-recognition algorithms that were developed at Britain's Joint Speech Research Unit, in Cheltenham. Both systems are based on template-matching technology: Marconi's SR-128 is a dedicated speech-controller, while Logica's Logos is more of a general-purpose system and has a modular multiprocessor architecture.

Logos matches at the word, rather than at the phoneme level. Words spoken singly are compared with stored-word templates, while phrases are recognized by stringing likely word templates together and selecting the syntactically best sequence. Logica's approach is designed to handle connected words, something that many systems cannot, because it does not need to locate word endings. Extra processing power is needed to test all word-string combinations.

In more detail, connected speech is recognized by carrying out a spectral analysis in real time. Voice energy in 13 different speech bands is determined from sample to sample and stored to build up a complete fingerprint of the phrase to be recognized. Differences in rates of utterance are compensated for by dynamic programming. With Logos, the user can set up syntactic rules to adjust the active vocabulary to match the context and so improve the speed and recognition performance.

Logos is highly modular and can be configured with up to 10 Intel 8086s. The system's vocabulary can be extended from 120 to 2,000 words simply by adding memory. At any given time, the active vocabulary can handle up to 300 words. At this writing the SR-128 has a vocabulary of 240 words. **–K.S.**

BUSINESS AUTOMATION

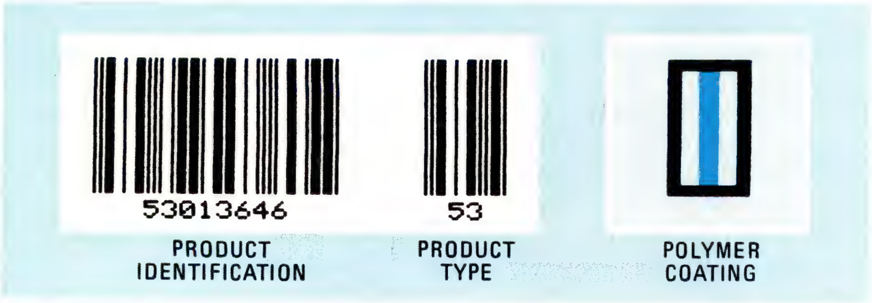
COMPUTERS AND POLYMERS CUT PRODUCT SPOILAGE

Morristown, N.J.—Distributors of such perishable products as foods and pharmaceuticals often lose significant amounts of money when their goods spoil before they reach retailers. But a new system from Allied Corp. that blends temperature-sensitive polymers with electronic technology could eliminate many of these losses.

Allied's Lifelines Inventory Management System employs a hand-held computer and a line of temperature-sensitive bar-code labels that are affixed to shipping cartons for scanning with an optical wand. The computer displays the percentage of the product's life cycle remaining.

The system not only helps to do away with much of the work now involved with the shipment of time-critical goods—such as stamping merchandise with dates—it also provides an alternative to unreliable methods such as squeezing products to ascertain freshness.

"You're no longer at the mercy of people. The judgment changes to quantitative analysis," says J. Tait Elder, president of Allied's New



Chameleon code. A polymer that changes color is added to a standard bar code as part of system that monitors age of perishables.

Ventures Group here, which developed the system.

The group was set up as a separate operating company several years ago to serve as a liaison between Allied's research and marketing departments. "We have had diligent research and a good patent effort for decades. We decided our technologies have got to have uses for other than Allied Chemical," notes Elder. In the case of the Inventory Management System, he says, "New Ventures' contribution was as much drawing everything together as developing the polymer."

The proprietary polymers used in the bar codes change color based on the length of time a product has been exposed to a certain temperature. For example, one polymer changes to a deep blue as a shipment of bananas ripens.

Bar codes use polymers suited for either ambient, chilled, or frozen products. To read the bar code and polymer, the computer runs a program designed by Allied that also provides such assessments as "product good," "discard now," and "ship immediately."

The computer has 80-K bytes of memory and can operate on either 115 V ac or on rechargeable batteries. The system, which also includes an interface to an IBM Corp. Personal Computer for data analysis, can be integrated into existing inventory control systems.

Years of work. The system's software enables the programming of a time- and temperature-tolerance curve for each product, and enables statistical correlations to be made between readings from the bar code and product-quality measurements. "It took a few years of man-hours—a heck of a lot of work to implement something we understood how to do," says Elder.

Based on market research conducted by Allied, Elder thinks it's a very promising area. He feels that the main reason the concept will fly, in addition to reducing product spoilage, is ego-based: distributors are image-conscious businessmen who strive to be known for carrying fresh goods.

Allied expects the system to reach the market early next year. The introductory price of a complete custom-designed evaluation system will be under $20,000. After an initial free shipment, the labels for shipping cartons will range in price from 15¢ to 75¢, depending on volume.

The company, which is now testing the system in a dozen locations, has high hopes for its product. "Testing so far has been very smooth," says Elder, who admits to a few minor problems, such as bar codes picking up stray light, a situation remedied by putting a filter over the wand. "Eventually it will be a $50-million-a-year business. If we didn't think so, we wouldn't have tackled it," Elder notes. **–Steve Haggerty**

BUSINESS ABROAD

ELECTRONICA EVOLUTIONARY, NOT REVOLUTIONARY

Munich—Hardly anyone who is familiar with the electronics business visits an exhibition expecting to be awed by what is claimed to be a "radically new development." Instead of revolution, showgoers are more likely to witness an evolution of technology, refinements of or improvements on what existed before.

It was no different at the biannual Electronica show which, after a five-day run here, closed its doors Nov. 17. To be sure, virtually all of the nearly 2,200 exhibitors from Eastern and Western Europe had interesting products on display—from electromechanical and optoelectronic devices to sophisticated microprocessors and memories. But most of the approximately 90,000 visitors who crowded the 19 exhibition halls at the Munich Fairgrounds saw products and developments that underscored ongoing trends and answered the question of where electronic componentry is headed.

One of the major trends that Electronica spotlighted this year is the use of surface-mounted devices, which played a prominent role on the stands of scores of companies. SMD technology appears to be making headway not only in entertainment electronics, where it started, but into virtually all sectors of industrial elecronics: office and data equipment, communications gear, automotive electronics, and measuring and control systems.

Coming on fast. The technology is coming on the scene much faster than at first expected. Experts at Electronica forecast a 15% to 20% growth in the use of surface-mounted components by European companies for next year and by 1990, they say about half of all the components are likely to be SMDs. Philips, of the Netherlands, a heavyweight in SMD technology, estimates that worldwide annual shipments of parts for surface-mounted assembly will reach 30 billion by 1985 and 80 to 100 billion by 1990, which amounts to about 25% and 50%, respectively, of all components shipped.

The Dutch company itself introduced a line of modular automatic-placement surface-mounting machines boasting assembly rates of up to half a million components an hour, in addition to a line of surface-

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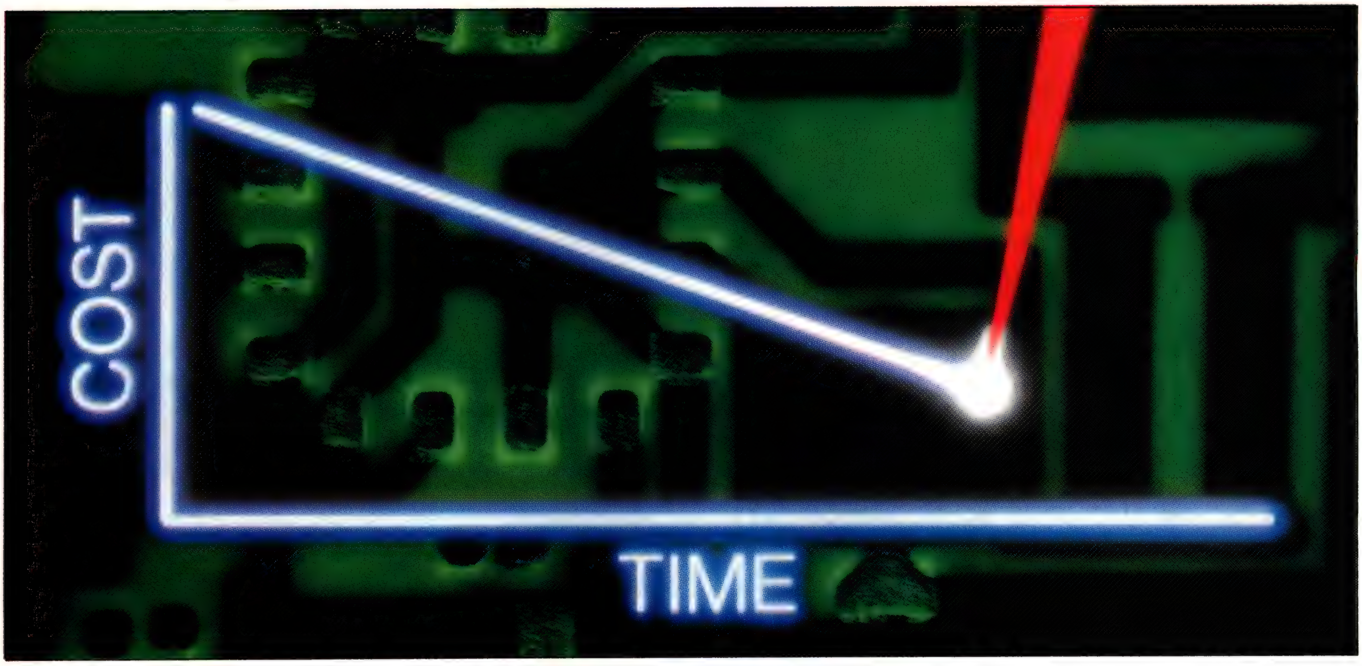

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Engineers at GTE Microcircuits are happy too, and this may be the highest tribute to the experiment's success. They've found their technological base broadened. Working together with Eaton engineers, they become more familiar with joint challenges and

"When we approached Eaton we were looking for a partner."

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Another trend much in evidence at the Munich show was the rapid changeover from mechanical, electrical, and electromechanical sensors to semiconductor types. Semiconductor sensors fulfill all requirements imposed on sensors for industrial-scale applications: they are reliable, stable, accurate, small, and lightweight. Furthermore, with the semiconductor industry already using automated production techniques for other components, semiconductor sensors can be made at low cost.

Semiconductor pressure sensors have been around for some time, but are now beginning to come integrated on the chip that processes their output. One important field of application for such monolithic pressure sensors will be in automobiles to measure, for example, the pressure in the carburetor intake pipe in order to optimize the ignition timing, or for accurate and reliable fuel level indication.

At present, temperature sensors outsell all other kinds, but are outpaced in dollar value by the relatively high-priced pressure sensors. The respective shares of the total sensor market for temperature and pressure sensors are 25% and 39%, respectively. Position and movement sensors check in with 13% and other types with 23% of the total sensor business, according to Philips.

Graphics growing. Much is also happening in the area of graphic display chips. "General computer awareness is growing fast and everyone wants graphics capability with his personal computer," says Francis Marx, product and marketing manager for display products at Thomson-CSF. "By 1986 virtually every machine sold will feature graphics."

On its stands at Electronica, the Thomson Semiconducteurs division of Thomson-CSF showed off its running start on what it reckons will be a gigantic market in a couple of years. New offerings include products aimed at adding graphics capabilities to mid-range and low-end terminals, work stations, and personal computers.

In addition to the single-chip semigraphic display processor and single-chip color palette, Thomson has also sown the seeds of interest in the next generation, which is scheduled for production next year—a monolithic graphic display processor that combines both of these functions with a host of other options.

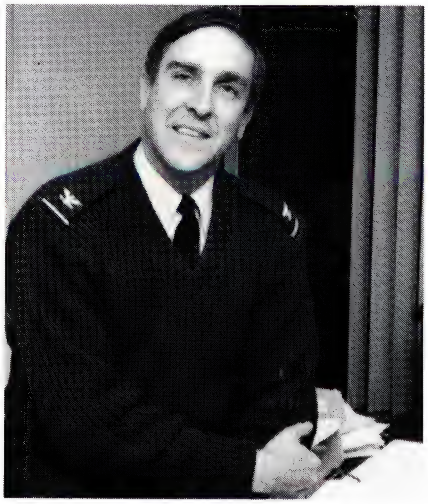
The circuit on which the Paris company is betting most heavily is its EF9369 full-graphic-display bit-map processor, a circuit that Marx predicts will run into heavy competition, as he expects virtually every major IC house to be vying for a piece of that multimillion-dollar chip market. Thomson expects to make its official product announcement in the first quarter of next year and to begin shipping samples no later than the third quarter. **–John Gosch**

RADAR

JOINT STARS FLIES AGAIN

Hanscom AFB, Mass.—The on-again, off-again Joint Surveillance and Target Attack Radar System development program is on again. A second round of proposals for the system, which is designed for use by both the Army and Air Force, is due to be received later this week.

Joint Stars is a multimode synthetic-aperture radar system for the detection and tracking of stationary and slow-moving targets. Although more than $1 billion has already been appropriated for research and development, one of the primary challenges still confronting the system is to accommodate the different needs of the two services.



Airborne. Air Force Col. Harry I. Gillogly III stresses the C-18's survivability as a platform for the new-generation radar.

Needs vary. Fundamentally, the Army wants a system directed toward a shorter field of view than does the Air Force. Earlier plans called for different specifications and the use of different aircraft platforms for the respective services. Proposals on that basis were received earlier this year but were never opened, says Air Force Col. Harry I. Gillogly III.

During the spring and summer, the proposal went through a consolidation. In June, it was decided to mount Joint Stars on the same platform, a C-18—that is, a militarized version of a Boeing 707—for both services. Then in August, Gillogly says a decision was made to proceed with the building of four identical copies of the system for further testing and development.

Responding to concerns that the C-18 is vulnerable on the battlefield, Gillogly reports, "We had analyses that show the C-18 is as survivable or can be as survivable as any other platform."

Gillogly also says the earlier proposals to mount Joint Stars on two smaller airplanes made it difficult to satisfy the needs of both services with one system. By using the larger C-18, maintains Gillogly, "size is no longer a problem."

In addition to airborne equipment, Joint Stars includes ground stations and weapons interfaces. It will provide real-time detection in either moving-target indicator or synthetic-aperture modes. Deputy project director Army Col. G. Sidney Smith predicts the system will move the current generation of radar technology forward.

"This is the first attempt to take [multimode] and use it in this form and application," says Smith. "The others have been aimed at some other mode and were only incidentally capable of identifying moving targets. This one is designed to detect moving targets and incidentally look at stationary targets. So it's really the base design that's changing."

The schedule now calls for a contract award next spring and a complete development model in two years. **–Craig D. Rose**

COLLISION AVOIDANCE INTEGRATED WITH RADAR

Great Neck, N.Y.—As the International Maritime Organization requires large- and medium-sized ships to be equipped with Automated Radar Plotting Aid (ARPA) systems, integrated computer-based navigation has proliferated on the bridges of commercial vessels. Sperry Corp.'s Marine Systems Division has taken integration a step further by retrofitting a collision-avoidance system with enhanced predictive capabilities to its updated radar system.

The 340 CAS, Sperry's third-generation collision-avoidance system, is integrated with a radar indicator into a compact and environmentally sealed cabinet measuring 100 cm wide by 102 cm high. The system uses five microprocessors (three 16-bit Texas Instruments TMS9900s and two 8-bit Intel 8085As) and nine replaceable printed-circuit boards. Also included are a 16-in. display for bright processed radar video and a 9-in. alphanumeric display. Sperry says it has sold over 900 of its CAS II systems, its second-generation model, and 1,300 systems overall. The 340 CAS will reach the market in the spring of 1985.

Space saver. By integrating collision avoidance with radar, bridge space is conserved and ship owners save the cost of an additional display, explains Frank M. Soccoli, an assistant marketing manager with the Marine Systems Division here. Before, two radar displays and an ARPA display were needed to meet International Maritime Organization requirements, he explains. Sperry has not released prices for the 340 CAS, but Soccoli says it will be under $40,000.

Raytheon Marine Co., Manchester, N.H., which says it shares roughly half the worldwide market and two thirds of the U.S. market with Sperry, downplays the significance of Sperry's integrated system and says it and other competitors already offer it. Capt. John R. Millard, a Raytheon nautical adviser, notes that the firm introduced a comparable system called the Raycas seven years ago and has come up with two updated versions since. "It's a matter of choice," he asserts in comparing the two rival CAS systems.

Predicting danger. "It's like driving either a Ford or a Chevrolet," he says, adding that the two systems are "pretty much evenly matched." But if a difference between the two collision-avoidance systems exists, it may well be Sperry's Predicted Area of Danger (PAD) system, an innovation commercially available since 1972 but shunned by ship's pilots accustomed to the traditional vector method of collision avoidance used by Raytheon and others.

"There was resistance because no one understood PAD," says Soccoli. Though the 340 CAS does include the vector system, the PAD alternative "gives us a predictive capability we didn't have before." Designed primarily to help avoid congestion in sea lanes and port approaches, the collision-avoidance system's computers collect and integrate information from the ship's gyrocompass, radar, and speed log.

Based on a preselected closest point of approach, areas of potential collisions are then displayed as hexagons on the 340 CAS screen. A pilot can determine which PADs his heading marker intersects and adjust the ship's course and speed accordingly.

"Our approach is simple: stay outside of the PAD and you'll steer clear [of collisions]," says Soccoli. "What we've done is take the vector method and expanded the geometry." The system tracks up to 20 targets in a 36-mile radius, at closing speeds up to 80 knots.

Besides integrating it with radar, Soccoli says, the system's competitive advantages include ergonomic enhancements that are important on cramped bridges during intricate docking maneuvers.–**George Leopold**

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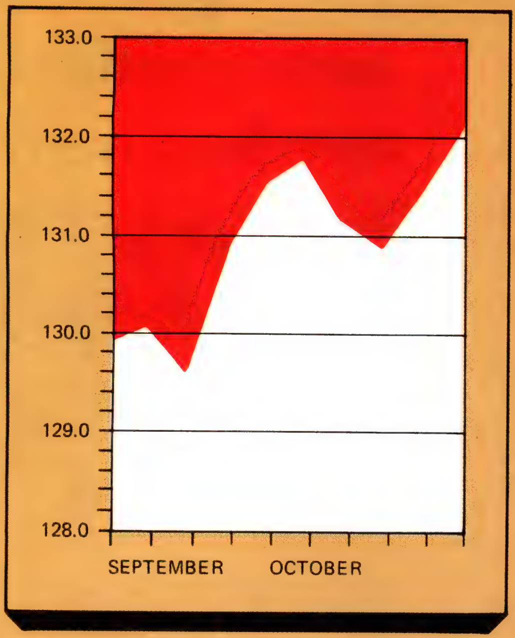
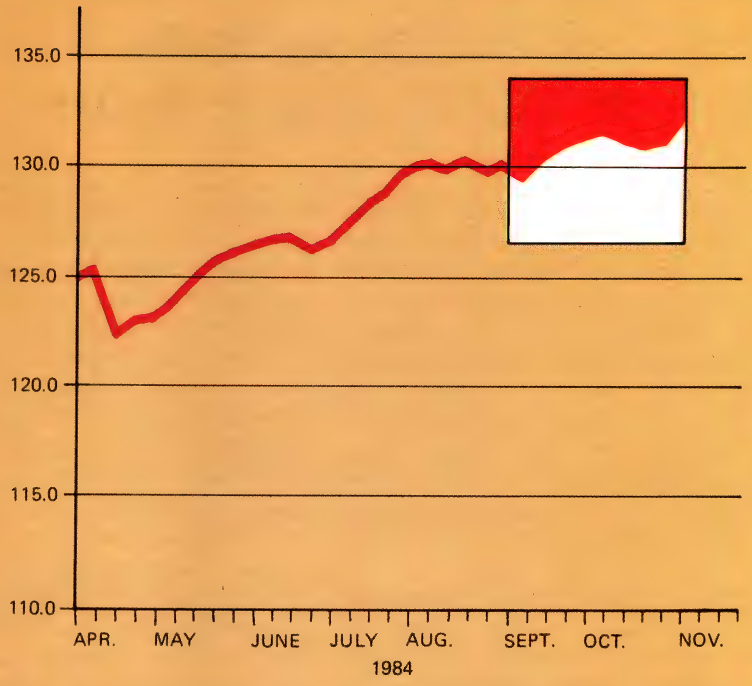
ElectronicsWeek Index



THIS WEEK = 132.2
LAST WEEK = 131.5
YEAR AGO = 98.5
1982 = 100.0



The *ElectronicsWeek* Index, a seasonally adjusted measure of the U.S. electronics industry's health, is a weighted average of various indicators. Different indicators will appear from week to week.

U.S. INDUSTRIAL PRODUCTION INDEX

Production workers (thousands)	September 1984	August 1984	September 1983
Office and computing machines	202.2	204.2	197.2
Communications equipment	288.2	285.3	262.3
Radio and TV receiving equipment	64.4	64.1	61.7
Components	427.2	428.1	361.6

Shipments ($ billions)	September 1984	August 1984	September 1983
Communications equipment	4.784	4.672	4.119
Radio and TV receiving equipment	0.841	0.881	0.721
Electronic and electrical instruments	4.882	4.746	4.297
Components	4.003	3.940	3.134

September's improved sales performance and slight gain in the employment of production workers in the electronics industry helped produce a 0.7% increase in the *ElectronicsWeek* Index for the latest week. Shipments of U.S.-made electronics equipment again showed their resilience in the face of a lackluster economy by booming ahead almost 23%, despite an overall weakness in the U.S. industrial sector. (In fact, the third quarter of this year was the weakest quarter for the economy since the recovery began, in January 1983.) Communications equipment, with shipments up over 16% from a year ago, remains the fastest-growing segment of the U.S. electronics industry, while shipments of radio and television equipment weakened.

Despite intense competition from foreign manufacturers of electronics equipment, employment in the U.S. electronics industry continued to grow. Nonetheless, some erosion took place in worker employment in the office equipment and component sectors.

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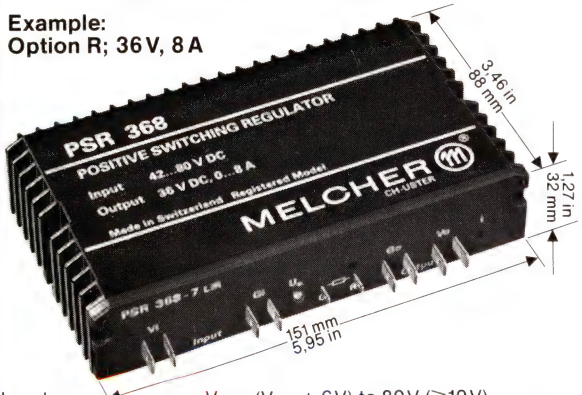

Input:	$V_{in} = (V_{out} + 6V)$ to 80V (≧19V)
V_{out} programmable:	PSR = 0 to +39V, NSR = −23 to −39V
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Output power nom:	288W (144W, 72W as well)
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Power density:	11W/in³ ≈ 673W/dm³
Efficiency:	95% typ.
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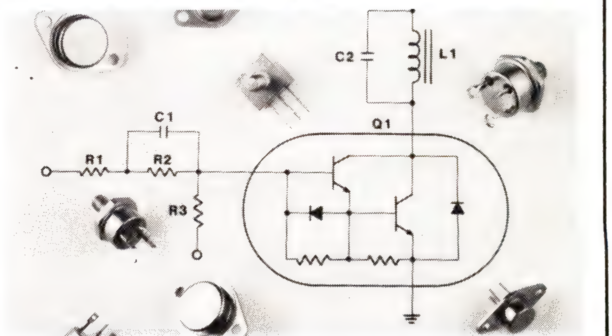

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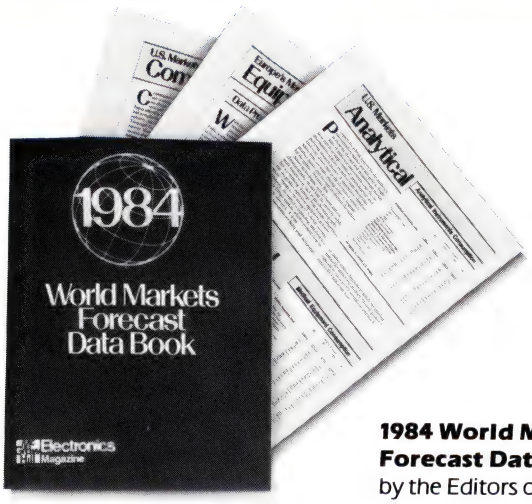

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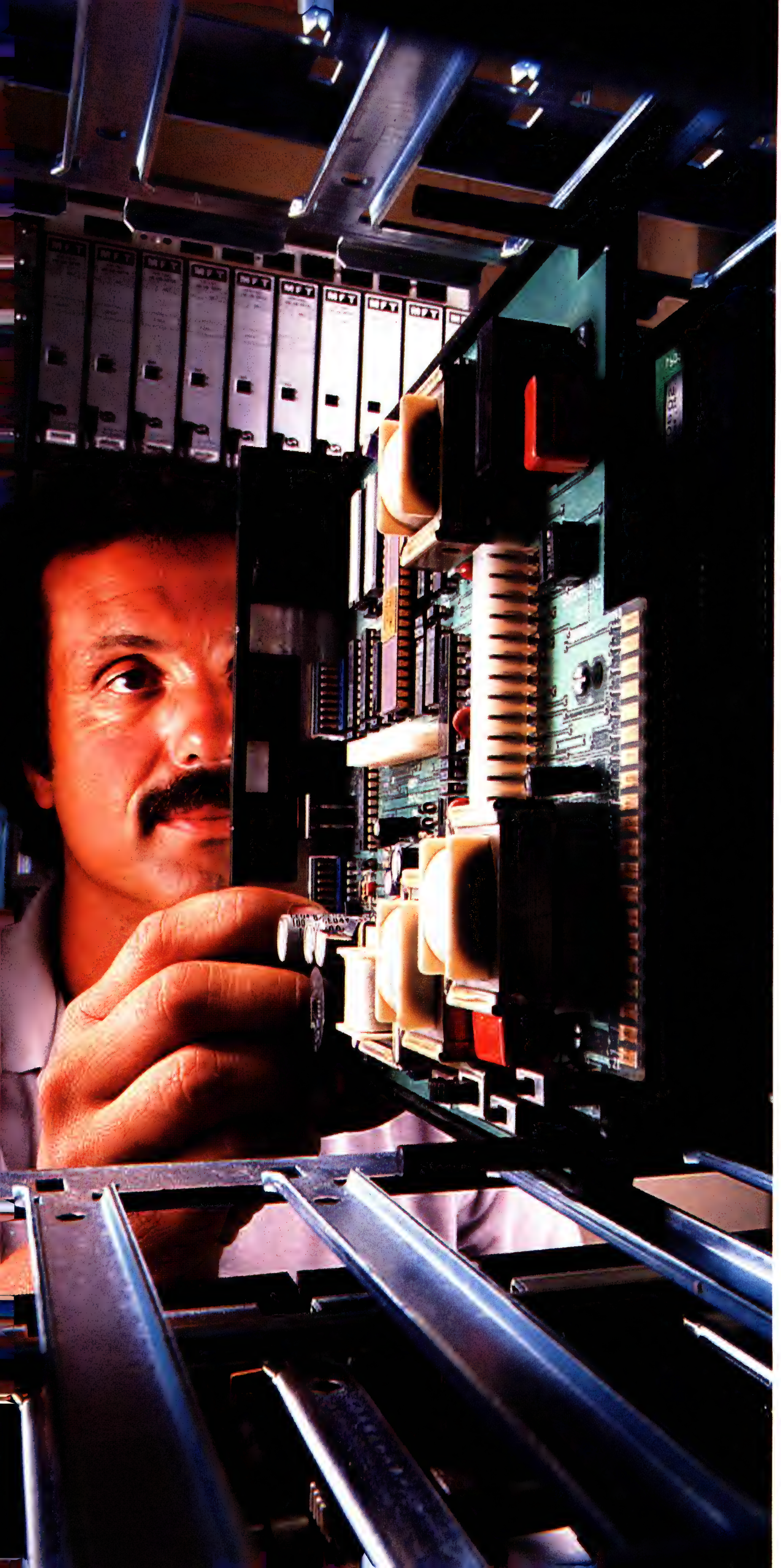
Texas Instruments digital signal processor helps Lear Siegler Inc. make your message loud and clear...from anywhere.

- **TI's single-chip, high-performance TMS32010** digital signal processor (DSP) assures highest quality telephone transmission *(Page 2)*.
- **TMS320 DSPs from TI** support high-speed and numeric-intensive applications from communications to seismic processing *(Page 3)*.
- **Complete development support** for TI digital signal processors includes hardware, software, documentation, and application workshops *(Page 4)*. ▶



TI digita distortio

When you're depending on the telephone to get your message through, y don't need "singing" on the line. A standard two-wire circuit "sings" wher signals traveling in opposite direction insufficiently isolated in a repeater. To eliminate this problem, Lear Siegler, Inc., manufacturer of repeaters used worldwide, relies on the Texas Instruments TMS32010 digital signal proce (DSP). And cuts setup time for each repeater from hours to minutes.

In the unique VFR-7608 repeater, TMS32010 performs all the function analog equalizers, filters, and amplifie (see diagram opposite). It compensate automatically for line impedance 8,00 times per second. Completely isolates opposing signal streams. Puts an end to "singing."

TMS32010 eliminates reflections "by the numbers"

The standard solution to "singing" is a analog network designed to cancel ou reflected signals on the line. But even with expensive "precision" hybrids, th best solution is a compromise that lim usable bandwidth and gain.

Digital signal processing with the TMS32010 balances the circuit across the entire frequency band every 125 Because the repeater adapts continuou the circuit *cannot* "sing" at any freque and its gain can be fully utilized.

DSP cuts setup time to minut

Tuning each analog repeater is an hou long, trial-and-error procedure for a highly skilled technician. Using a cor prehensive history of each circuit, he must set 68 switches in an analog repeater. TI's TMS32010 in Lear Sieg new digital repeater eliminates 65 of those switches. Ends the need to keep detailed circuit histories. And the sma affordable plug-in unit is interchangea with older repeaters.

So your message can always come through—loud and clear.

◀ **Setup is as simple as 1-2-3** with Lear Siegler's adaptive telephone repeater usin TI's TMS32010 DSP. Whereas manual adjustment of an analog repeater can tak many hours, only three simple switch set are required to assure rock-stable, "sing"- performance from the digital repeater.

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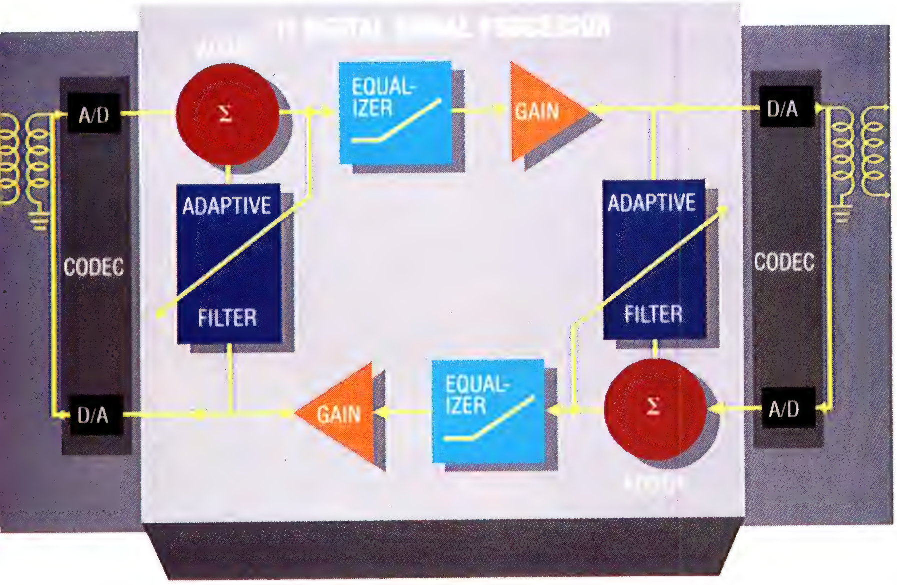
ignal processor squelches n unique adaptive repeater.



eart of the adaptive repeater is TI's single-chip, 16/32-bit TMS32010 digital signal rocessor. All the functions shown are achieved in real time through software operating on ignals digitized by conventional single-chip codecs.

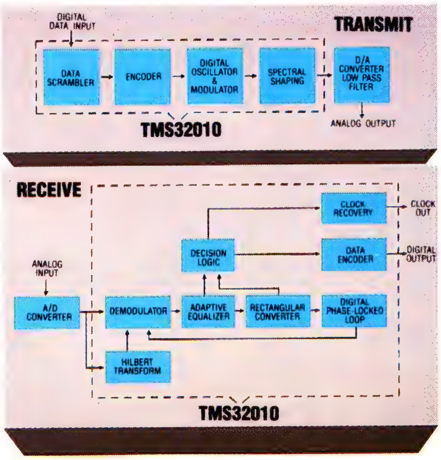
The TMS320 family from Texas Instruments: "Workhorse of digital signal processing."

The TMS32010, first member of the TMS320 DSP family, is TI's trailblazing ontribution to an important new technology. A Lear Siegler engineer who has een following the progress of digital ignal processing from its inception says, The TMS32010 is the first device that an reliably do what we need. It's a real vorkhorse: The '8080' of DSP."

TI's TMS320 DSPs xcel at high-speed, numeric-ntensive applications

igh-performance TMS320-family DSPs rom Texas Instruments will find widepread use in many fields where large olumes of high-speed computation are equired. In telecommunications, they an also be used to build high-speed nodems with data-transmission rates up o 9,600 baud. They can make speech ecognition, analysis, and synthesis practical. Speed image processing and pattern ecognition. Facilitate high-speed process ontrol and instrumentation. Process adar, sonar, and seismic signals. And urnish the multiple functions often equired for a single application.

For example, a TMS320 DSP could enable an industrial robot to synthesize and recognize speech, sense objects and their orientation, and perform mechanical operations through digital servo-loop computations.



High-speed modem functions are effectively performed by TI's TMS32010, as well as such expanded functions as auto-dial/answer, dial-tone verification, busy-signal detection, and self-test routines.

The TMS320 family, with its extensive development support *(see page 4)*, can handle all the signal processing for spectrum analysis: Autocorrelation, windowing, fast Fourier transforms—performing a 64-complex-point FFT in only 550 µs. And for seismic processing involving very low frequencies which only a digital system can implement.

Image enhancement, pattern recognition, and data compression are all possible with TMS320 processors. They can extract features and perform template comparisons for optical character recognition.

A one-chip alternative to bit-slice processing

TI's 16/32-bit TMS320 DSPs offer an inexpensive alternative to multichip bit-slice processors. They combine the flexibility of a high-speed controller with the numerical capability of an array processor—on a single chip, in one 40-pin DIP.

Highly pipelined architecture and a comprehensive instruction set give the TMS320 the speed to execute five million instructions per second with 32-bit precision: More than fast enough, for example, to handle the 40 additions and 40 multiplications necessary for realtime voice-frequency processing within the 125-µs sampling interval. A conventional microprocessor, operating at 8 MHz, would require 900 µs, and quickly become bogged down in the signal stream.

Now in three versions

The TMS32010 microprocessor has 288 bytes of on-chip data RAM, and can address up to 8K bytes of off-chip memory at full speed.

The TMS320M10 microcomputer is identical to the TMS32010, but it also includes 3K bytes of on-chip mask-programmed ROM.

The military version, SMJ32010JDS, is processed to the extended temperature range requirements of MIL-STD-883B.

To learn more about the many applications and available development support for TMS320-family DSPs, return the coupon on the following page.

See back page for more information.

XDS/22 Installation and Operation Guide
XDS Breakpoint/Trace
TMS32010 Evaluation Module
XDS/22 TMS32010 Emulator
TMS32010 Simulator
XDS TMS32010 Emulator Hardware
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Companding Routines
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TMS32010 User's Guide
TMS32010 Assembly Language Programmer's Guide
TMS32010 VAX/VMS Cross Support
TMS32010 IBM/MVS Cross Support
TMS32010 Development Support
Software Development System

In-depth support for the TMS320 family of TI DSPs includes a host-independent development system, an evaluation module, emulator and analog interface board, as well as assembler/linkers and simulators that can run on a variety of host computers and PCs. Documentation is extensive and thorough.

Develop your own DSP applications with comprehensive support from TI.

Texas Instruments has assembled an extensive group of development-support packages for the TMS320 family of VLSI digital signal processors (*see table*). Included are all the hardware, software, and documentation you need to utilize the power and speed of TMS320 DSPs in your designs. A rapidly growing volume of third-party support is also available.

TMS32010 Software and Hardware Support

Host Computer	Operating System	Part Number
Macro Assembler/Linkers		
TI990	DX10	TMDS3240120-08
DEC VAX	VMS	TMDS3240210-08
DEC VAX	Berkeley UNIX 4.1	TMDS3240220-08
DEC VAX	Berkeley UNIX 4.2	TMDS3240230-08
IBM	MVS	TMDS3240310-08
IBM	CMS	TMDS3240320-08
TI/IBM PC	MS-DOS	TMDS3240810-02
Simulators		
DEC VAX	VMS	TMDS3240211-08
TI/IBM PC	MS-DOS	TMDS3240811-02
Hardware		
Evaluation Module (EVM)		RTC/EVM320A-03
Analog Interface Board (AIB)		RTC/EVM320B-06
Emulator		TMDS3262210

Use your own PC as a TMS320 development station

The latest addition to TI's development-support software is the TMS32010 Digital Filter Design Package developed by Atlanta Signal Processors Inc. It makes your Texas Instruments Professional Computer or IBM PC a cost-effective, easy-to-use, digital-filter design station. With it you can produce the TMS32010 source module. Then you can assemble the code and simulate it in software on the PC. Later you can download the code into the hardware-development system for realtime emulation.

Two versions are now available: **DFDP-TI001** for the Texas Instruments Professional Computer, and **DFDP-IBM001** for the IBM PC.

Learn in TI workshops

Texas Instruments supplies comprehensive documentation with each device. A growing library of application reports will also assist you in the design of digital signal processing circuits using TI's TMS320 DSPs.

Three-day DSP workshops, including extensive hands-on experience, are conducted periodically at Texas Instruments Regional Technology Centers. For registration information, call the Regional Technology Center nearest you: Atlanta, (404) 452-4686; Boston, (617) 890-4271; Chicago, (312) 228-6008; Dallas, (214) 680-5096; Northern California, (408) 980-0305; Southern California, (714) 660-8164.

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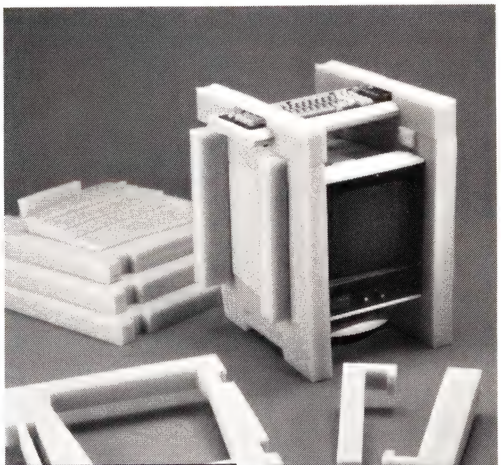

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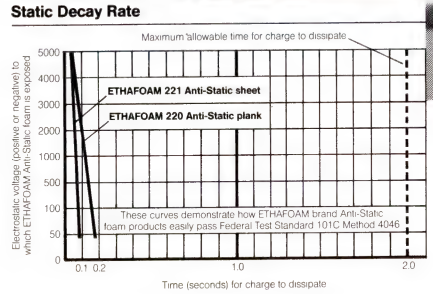
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A few ways you can take advantage of ETHAFOAM Anti-Static foams.

Cushion packaging applications—ETHAFOAM Anti-Static foams can be used to protect sensitive electronic devices from physical and electro-static damage during shipment. They can be made into corner blocks, braces, saddles, pouches, bags, envelopes, wraps, interleaving and encapsulating products.

Materials handling applications—Here ETHAFOAM Anti-Static foams provide a soft, non-abrasive cushion while protecting parts from static discharge. The foams can be made into trays or tote boxes, or they can be used as a lining inside those products. They can also be made into shunt (stuffing) boards and parts separators.

Work station accessories—In this application, these anti-static foams can be made into table and bench top covers, floor mats, seat cushions, and many other products for clean room environments.

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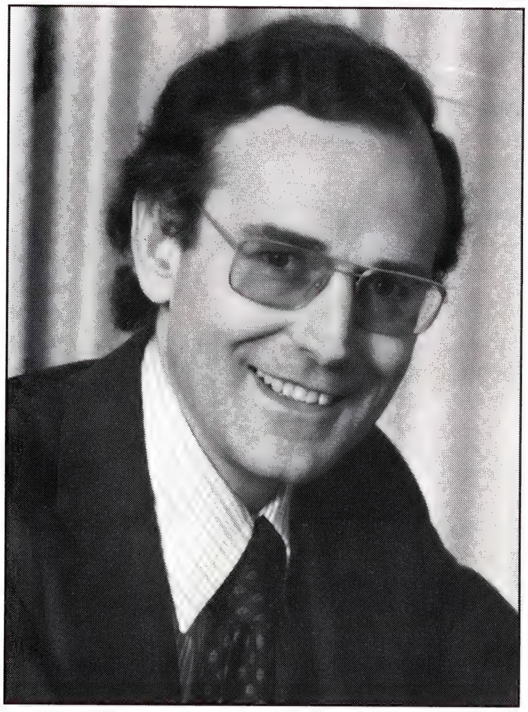
PEARCE ENVISIONS UMBRELLA ORGANIZATION FOR MARKETING

London

John Pearce can give two good reasons why small software companies should talk to him. First, as a veteran of Britain's software industry with two successful startups behind him, he understands their problems. Second, six months ago, he founded Pearce Technology Ltd. to help them move into worldwide sales.

Bankrolled to the tune of $3.6 million by British and U.S. venture funds, Pearce Technology plans to spend up to $12 million buying into small software outfits. Then it will set up the sort of worldwide sales and distribution outlets needed to turn good software products into best-sellers.

So far, the industry has responded enthusiastically, says Pearce: "We have received 55 other proposals since May." This month, Pearce Technology signed up its first client, taking a 20% stake in Reactive Technology Ltd., a London company that provides an on-line interactive service for users of Commodore International's 64 personal computers.



Connector. By buying into many small companies and linking with U.S. firms, John Pearce hopes to maximize both marketing effectiveness and information sharing.

Started with Hoskyns. His belief in the need for an international sales and distribution operation for British software stems from his first venture, the Hoskyns Group, which he cofounded with John Hoskyns in 1964. Martin Marietta Corp., in Bethesda, Md., a major user of Hoskyns software in the U.S., subsequently bought the operation, and Hoskyns moved on to become an influential adviser to Prime Minister Margaret Thatcher. Most recently, he became director-general of the Institute of Directors, a powerful lobbying body.

Pearce, meanwhile, was absorbing the lessons of this first successful venture and planning to repeat it. "I learned then that you had to be prepared to make a big up-front investment and look to recoup it, long-term, in the U.S. market," he says.

In 1979, the government-funded British Technology Group formed Aregon Ltd., with Pearce as its managing director. In May of this year, Pearce Technology Ltd. bought Aregon from the group. After a slow start, Aregon is now heading for success as one of the world's leading suppliers of videotex software; the firm employs 75 people and expects 1984 sales to hit $5.76 million. Since re-entering the private sector, it has inked a collaborative agreement with AT&T Co., New York, to develop a new generation of videotex software that can support U.S. and European standards as well as keyword searching and other fancy facilities.

Pearce has also formed a peripherals company to market the Excom 100 text and graphics work station, formerly marketed by Aregon.

With these activities, Pearce plans to replay a concept, developed under the previous government, of an umbrella marketing organization. He reckons that the basic idea was never really given a fair chance. "The problem was to use short-term capital in a long-term venture," he points out. Now, by taking a long-term stake in those companies whose products he will market, Pearce will be able to put his ideas to the test. First of all, he wants to tie up with companies in the UK. But later he expects to link with U.S. companies, too, and establish a two-way flow of software.

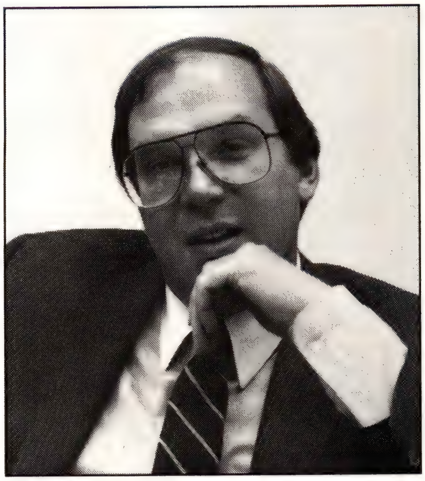
–**Kevin Smith**

AT&T's Crume in Japan to solve Unix differences

Tokyo

His new position as director of Unix systems, Japan and Pacific, which he assumed in mid-July, represents a big career change for Larry L. Crume. After 18 years at Bell Laboratories in the U.S. developing computer and communications applications, he is now responsible for all business and all technological development related to Unix in his area. Moreover, his mandate includes replacing himself here at the end of two years with a Japanese person and one or more persons in his other territories: Australia, New Zealand, Taiwan, Korea, Singapore, and India.

At the outset, he must supervise the creation of a Japanese language version of Unix, and for this Crume has a proven track record. From



Negotiator. Larry L. Crume must get consensus among Japanese Unix licensees to ensure their versions are in sync with U.S. ones.

1981 on he was Unix system manager at Bell Labs in Murray Hill, N.J., with the responsibility of planning and producing Unix System V. About a year ago, the job was split because it had become too big for one manager, and Crume was given the planning spot.

In April, while he was still working for the Labs, Crume spent two weeks visiting major Unix users in Japan. He found that their Japanese language extensions of Unix were noncompatible and inconsistent. He also found that the Japanese licensees wanted AT&T to take a more active role in developing a standard Japanese-language version of Unix. The proposal that he made on his return for a strategy for the Japanese market led to his being selected for his present position.

To help him in his task of creating a Japanese-language version of Unix, Crume has assembled an advisory group of experts from major Unix users, including the University of Tokyo, Nippon Telegraph & Telephone Public Corp., and several large Japanese manufacturers.

Travelin' man. A big problem for Crume will be getting a consensus from the Japanese licensees. To ensure that Japanese and U.S. versions stay in sync, he will make quarterly trips to confer with developers in New Jersey. He will also travel to the U.S. to attend meetings of the board of the International Network of Unix Users, called /usr/ group, to which he was elected this year to represent AT&T.

Crume says that his talk at the Uniform conference next January in Dallas will publicize Japanese work in Unix, which he feels will be beneficial to Japanese licensees. He will also travel in the Pacific area to meet licensees or potential licensees, attend to their needs, or negotiate licenses.

Although he emphasizes his new position is a move away from engineering toward business, Crume actually concluded several business deals with customers while at the Labs—helping, in the process, to get him elected to the board of the /usr/ group.

–Charles L. Cohen

Tapping Soviet TV starts inventor's dream

New York

Alternately lounging and pacing in his Manhattan apartment that doubles as the headquarters of Orbita Technologies Corp., inventor and philosopher of science Ken Schaffer talks expansively about what he sees as the failings of the engineering establishment and how he plans to beat it at its own game. Referring to his current interest, satellite receiving systems, Schaffer makes no bones about his intentions: "I want to be the Johnny Appleseed of this technology." he proclaims.

Schaffer, 35, has received considerable attention here recently for accomplishing something the engineers—Schaffer emphasizes he is not among them—said couldn't be done: the installation of a satellite dish capable of receiving television signals from the Soviet Molniya satellite system in a high microwave-interference site on the island of Manhattan.

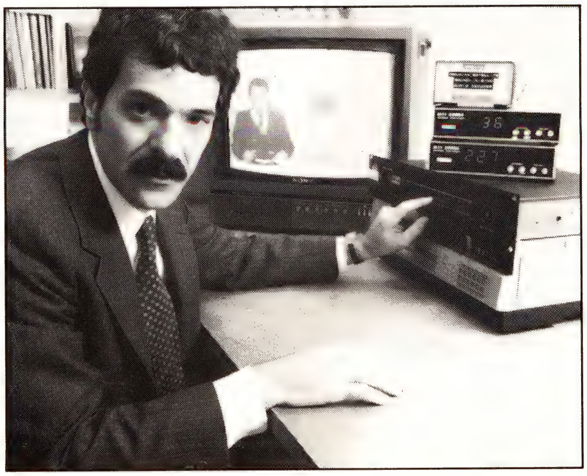
Schaffer spent three years researching and developing the data and equipment needed for the project, housed at Columbia University's W. Averell Harriman Institute for Advanced Study of the Soviet Union. He developed a computerized system for 24-hour tracking of Soviet satellites oriented in highly inclined elliptical orbits around the poles, and processing Soviet signals radically different from U.S. linear signals.

Against the grain. "I've been doing things against the advice of well-intentioned engineers" for a long time, says Schaffer. The computer-steerable, 11-ft dish antenna was installed in late September, and has been providing what Columbia officials call sharp color pictures and clear sound from Moscow's Programma I network.

A native New Yorker, Schaffer studied the philosophy of science at the City University of New York in the 1960s and later became a successful music publicist. With an interest in music and his self-taught electronics skills, he later developed a wireless electric guitar and perfected a wireless microphone widely used today by the music and recording industries. In 1977, he formed the Ken Schaffer Group Inc., whose clients included several well-known musical groups, the National Aeronautics and Space Administration, and Bell Laboratories.

In 1982, he produced a "live by satellite" climb of Mt. Everest for the American Broadcasting Co. "I'm selling live video now," Schaffer explains. "Who wants yesterday's paper?" Earlier this year he formed Orbita Technologies as a marketing base for future projects. Schaffer, who calls satellite antenna technology the ham radio of the 1980s, says agreements with four other universities and two foreign embassies will be announced soon.

–George Leopold



Inventive. Ken Schaffer developed a tracking system to monitor Soviet television despite skeptics who said it couldn't be done.

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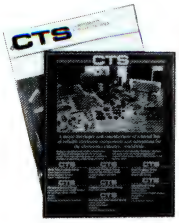

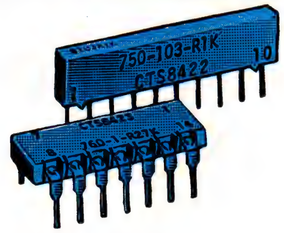

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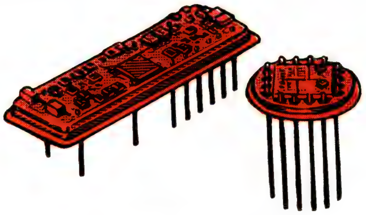

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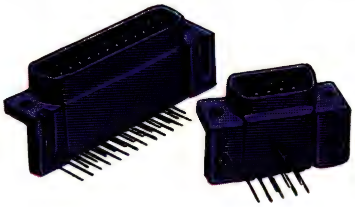

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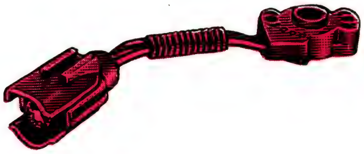

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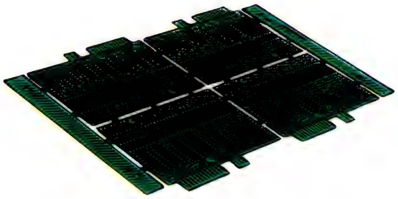

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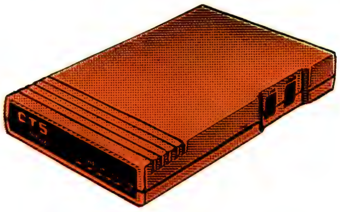

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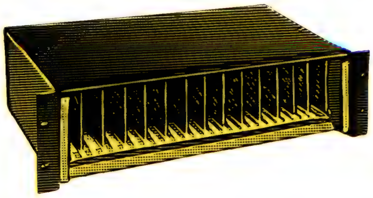

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PRW

CULLINET PARLAYS SOME BASICS INTO THRIVING BUSINESS OPERATION

Westwood, Mass.

A Horatio Alger scenario might call for a hard-driving leader with a revolutionary idea to lead a company through a long trail of red ink to ultimate profitability. But that storybook quality does not seem to pervade the history of Cullinet Software Inc., where a self-described nine-to-fiver has parlayed some basic ideas into what has become both steady and spectacular success.

Cullinet has become the largest independent software company in the world by selling data-base-management systems and related tools for use on IBM Corp. mainframes. Its success can be viewed as the blossoming of two fundamental ideas: first, that a business based on packaging and selling software could be profitable and, second, that all new products would be integrated with existing products.

Cullinet (which was originally called Cullinane) was founded in 1968 as one of the first independent software companies. The company's profitability was by no means an overnight success story, recalls John J. Cullinane, founder, former president, and now chairman of the board. On one particular day, he recalls, "We had only $500 in the bank and an $8,500 payroll due. An $8,500 check came in that day."

Cullinane did his early learning about the computer business while he was a cooperative student at Northeastern University in Boston and working at management consultant Arthur D. Little Inc. To maintain his family life, he says he has purposely kept the business on a mostly nine-to-five schedule. Those have been productive hours. In the past four years, revenues have increased at more than 50% annually to more than $120 million, with profits rising to more than $24 million.

By 1973, Cullinane says, his firm reached a modest level of success based on its report writer and auditing software. But then he decided to go sell DBM systems. "It was a bet-your-company decision," he says. "At that point, data base had a bad reputation—it was enormously complex, would require a lot of people, was difficult to sell, you'd be coming in direct head-to-head competition with IBM.

"There were a lot of potential problems, but we had the good fortune to acquire an outstanding product [a DBM system from B.F. Goodrich Co., Akron, Ohio] that we were able to cope with very nicely. It was very efficient, but we still had to do a lot of enhancement and rewrite. The system of 1974—you wouldn't recognize it today."

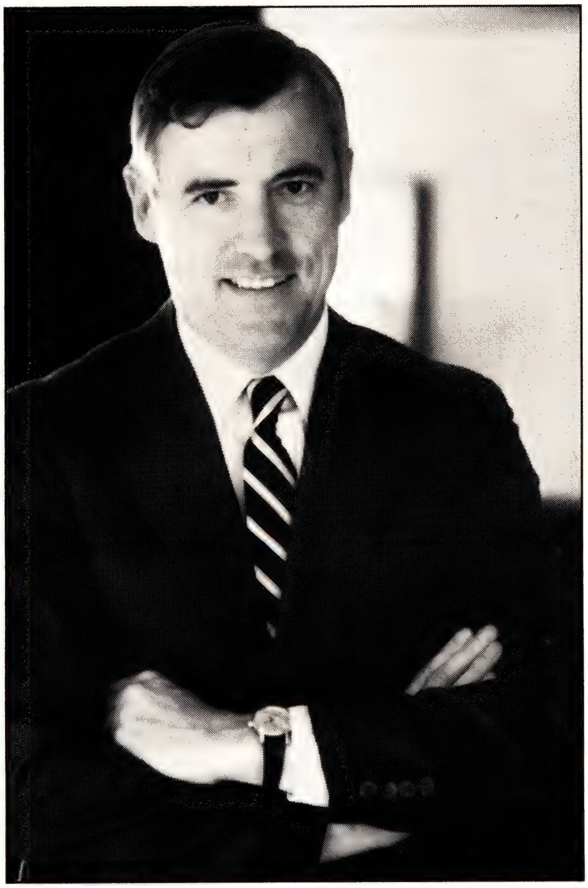
The business of DBM systems has changed as well. Although Cullinet claims some 2,000 installations of its DBM systems, add-ons such as application-development systems and end-user tools probably account for more revenue than the basic data systems themselves.

Specific applications. Cullinet, along with other vendors in the business, is also moving aggressively into the application-specific area, most recently into the banking-applications market. In the last two fiscal years, the sale of integrated application systems jumped from 3% to 13% of Cullinet's revenue. Within five years, Cullinane says, applications should account for 50% of the company's revenues.

Specific applications are a natural growth area for a company that wants to offer a total integrated solution, he says. Others assert that such a move has become essential because of an inevitable counterattack in the DBM business itself—an attack many expect will come from IBM.

"IBM has a great incentive to capture data-base management," says Curt Monash, a vice president and analyst at Paine, Webber, Mitchell, Hutchins Inc. in New York. Because DBM has implications for system hardware, says Monash, "IBM will continue to do things in hardware to maintain account control."

Monash believes the IBM efforts could take any number



Expanding. The application-specific area is a natural growth area for a company that wants to offer a total integrated solution, says Cullinet Software head John Cullinane.

of forms—including the introduction of a DBM machine—but IBM will probably only gradually increase its market share. "Any specific physical function [such as DBM] will be likely to end up in hardware eventually," he says.

This is not to say that Monash foresees trouble ahead for Cullinet—quite the contrary. "They have the broadest and best-thought-out product line of any company in the software business," says the analyst, and he expects its growth to continue rapidly in the future. But he believes the growth will come from areas other than data-base systems.

Cullinane, on the other hand, says the company could "prosper doing data base for as long as I can see." IBM has always been active in the DBM business, he maintains, and any adjustments it might make would do little to affect Cullinet's business.

Head to head. As for competing head-on in writing software, Cullinane says, "IBM has no inherent advantage over us in the software business as they do over hardware companies. It takes, in our view, four outstanding system programmers, plus someone to document what they're doing, to develop some piece of software.

"That law applies to IBM as it does to us. So the more people you add to the equation the less efficient you become. IBM can't address that with money and people."

Cullinet now offers Goldengate, a six-piece software package for the IBM Personal Computer; it is designed to compete with packages such as Lotus 1-2-3. But most industry analysts suspect that Cullinet's foray into the PC-software market will remain relatively passive for the time being. "They're testing the waters," says Terence Quinn, an analyst with Dean Witter Reynolds Inc., in New York.

As Cullinet comes off a heavy schedule of product development, which in addition to Goldengate saw the introduction of a relational DBM system and a PC-to-mainframe link, analysts agree that the firm should be in for more healthy growth. Quinn expects 40% annual growth in earnings and 50% annual increases in revenues for the next five years. **–Craig D. Rose**

Franco-American chip firm's fortunes come out of the woods

Nantes, France

After what could only be called a difficult infancy, five-year-old Matra-Harris Semiconducteurs is ready to start growing. According to president Guy Dumas, operations of the joint venture of Matra SA, Paris, and Harris Semiconductor of Melbourne, Fla., broke even in July and will operate in the black for the rest of the year, leading to its first annual operating profit.

If the road to profitability was a rugged one, it was admittedly not all Matra-Harris's fault. In hindsight, there could not have been a more inopportune moment than during 1979 to launch a European integrated-circuit manufacturing house. But the fledgling Matra-Harris weathered the storm of the most severe recession in recent memory by sticking doggedly to its initial strategy of filling those market niches that demanded high-performance ICs in high volume and using Harris's CMOS process to produce the parts.

The firm's sales this year will total approximately $40 million, up from almost exactly half that figure last year, with sales concentrated in high-speed static memories and microprocessors. Dumas predicts sales will climb about 75% next year, to more than $175 million by 1988. That growth will be accompanied by an evolution in the firm's product mix.

Good news. Five-year-old Matra-Harris Semiconducteurs will be able to post its first operating profit this year, says its exuberant president, Guy Dumas.

Matra-Harris has access to microprocessor designs through its joint venture with Intel Corp., Santa Clara, Calif., and the firm's design center, called Cimatel, which is also based here. Microprocessors accounted for some 10% of the firm's turnover last year, although volume production of the 8051, 8031, 8086, and 8088 circuits and their CMOS counterparts propelled Matra-Harris's microprocessor business to approximately 27% of its total operations in 1984, a figure that Dumas sees growing as high as 50%.

Expanding line. Other changes will be a significant expansion of the company's gate-array business, now a year old. Already, its customers have completed 150 designs and the company will expand its line early next year from its current ceiling of 1,200 gates to 5,000 gates. A parallel effort will get it more deeply involved in dedicated telecommunications circuits.

Matra and Harris are happy enough with the result to have decided to invest another $25 million each to double their joint venture's production capacity between now and the end of next year. This will take the venture's total production to some 180,000 5-in. wafers per year.

"I know the current conventional wisdom is that to make real money in electronic components, you have to supply the broadest possible range of products," according to an industrial analyst at one of France's largest banks. "But personally, I find it difficult to fault Matra-Harris's strategy of trying to find the right niches while relying on the support of very strong partners. At any rate, you've got to give them credit. Profits in ICs by French companies are rare enough by any measure." **–Robert T. Gallagher**

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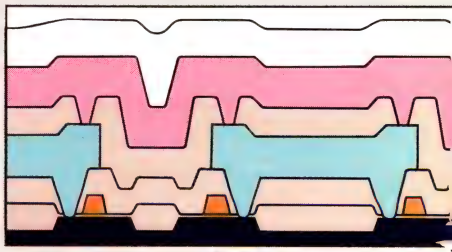

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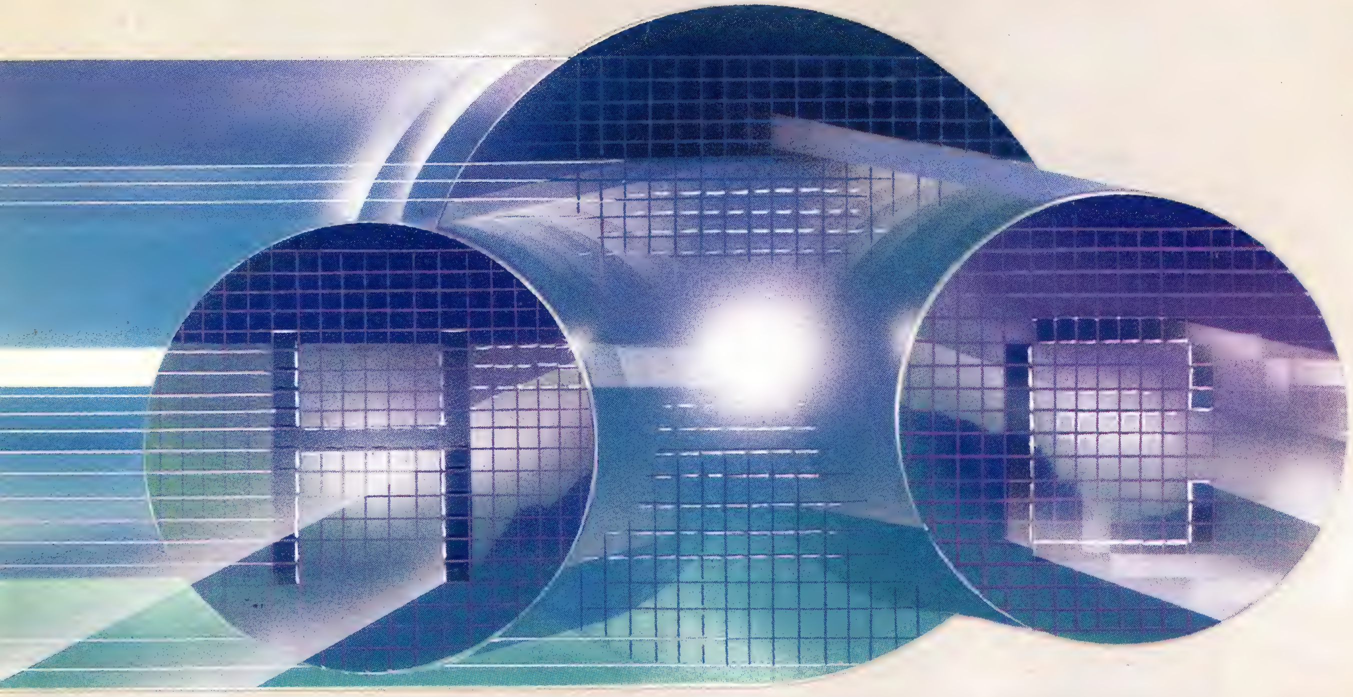

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High speed applications.

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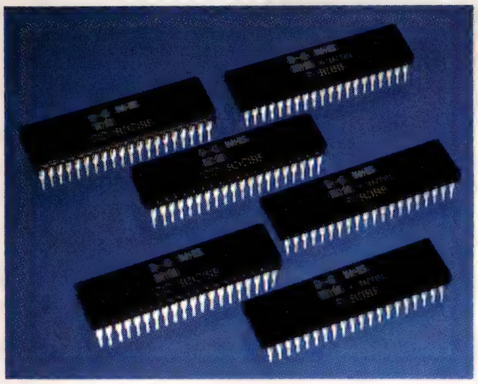

The 80C88, 5 MHz CMOS.

Fully compatible with its HMOS stablemate, the 80C88 (second source Harris) introduces a new fully/static design giving very low standby drain. MHS alone in Europe offers this benefit today.

High reliability applications calling for low power consumption.

The exceptional performance of the 80C88 makes it a prime candidate for the professional EDP market (portables), military and aerospace applications (on-board computers, fire control systems, field test systems).

8088 charateristics

8088/5 and 8 MHz	Temperature	Packaging
	0 to 70 deg C	DIL, PLASTIC, CERDIP
	-40 to +85 deg C	DIL, PLASTIC, CERDIP
	-55 to +125 deg C	DIL, CERDIP

80C88 charateristics

80C88/5 MHz	Temperature	Packaging
	0 to 70 deg C	DIL, PLASTIC, CERDIP *LCC, PLASTIC, CERDIP
	-40 to +85 deg C	DIL, PLASTIC, CERDIP *LCC, PLASTIC, CERDIP
	-55 to +125 deg C	DIL, CERDIP *LCC, CERAMIC

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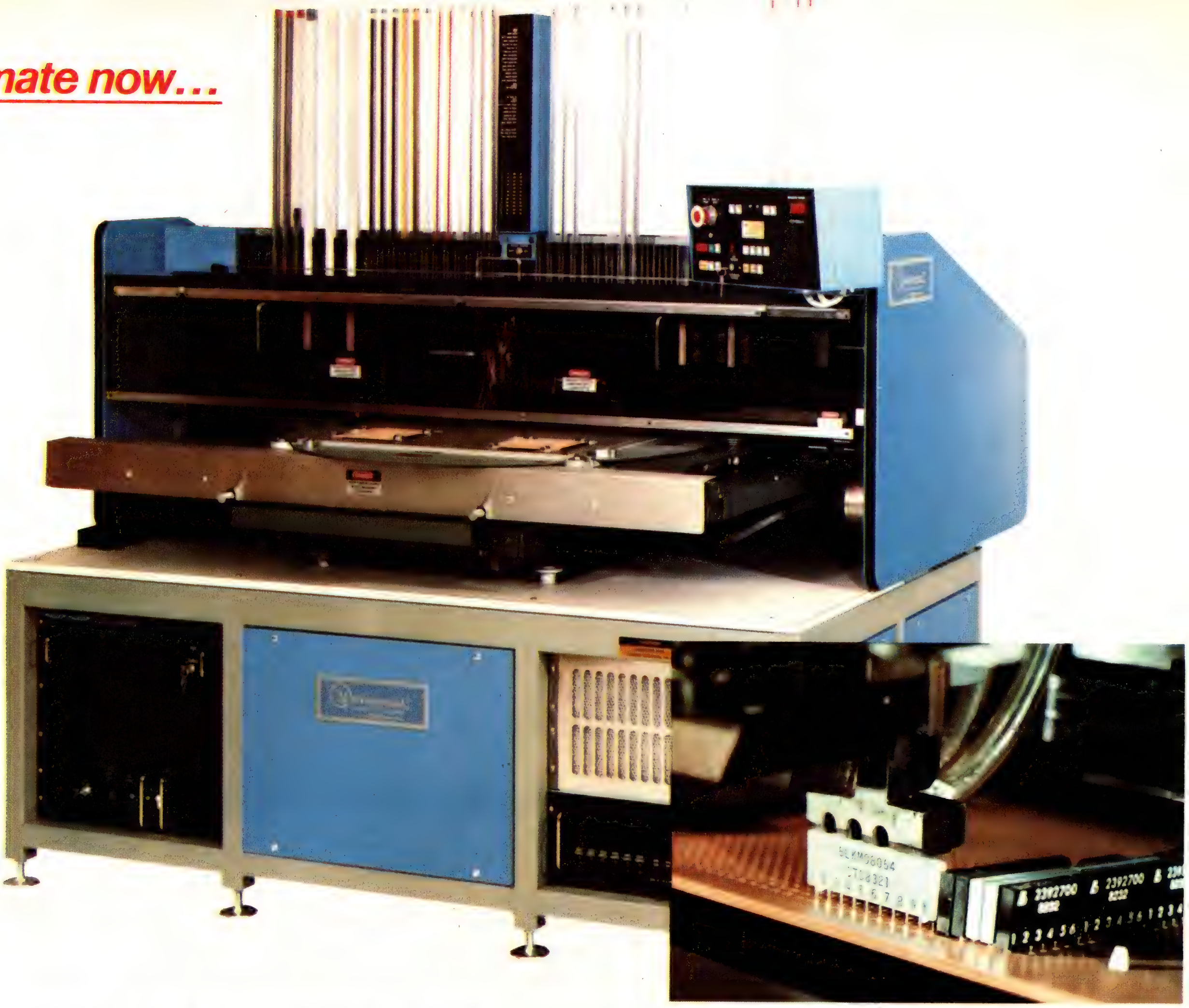

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SPECIAL REPORTS

DIGITAL SIGNAL PROCESSORS: DOING MORE WITH LESS

Rising interest in new applications brightens future of digital signal processing, and CMOS is helping

☐ *by Terry Feldt*

The quickening pace of single-chip digital-signal-processor introductions points to the day when DSP applications will mushroom, much in the way that microprocessors were instrumental in driving the computer invasion all the way to the desktop. A large market is expected—this is the carrot for chip houses, which hope that general-purpose digital signal processors eventually will find applications in communications systems of all kinds.

Many firms already produce digital signal processors; TRW, General Instrument, and Integrated Device Technology all plan to join the list. Driving the new uses of the chips, however, is the ever-growing demand for high-quality and price-competitive products and services—the stick for network vendors, communications carriers, and their suppliers.

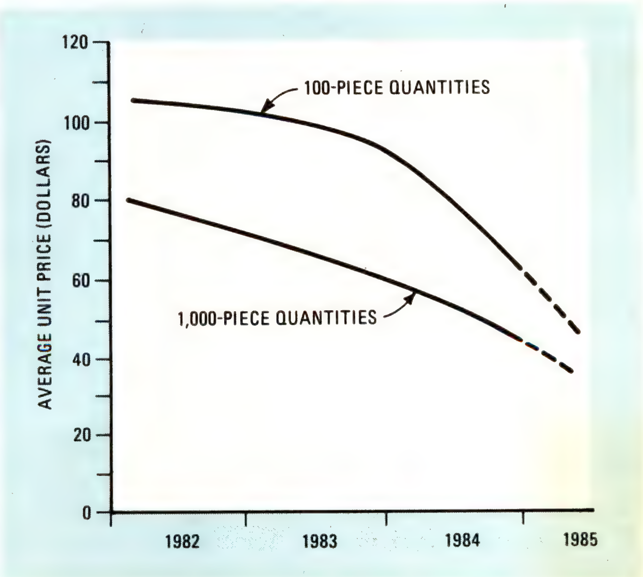
Led by the earlybird companies—Texas Instruments Inc. and NEC Corp.—these processors have demonstrated that they can fill the gap that exists between conventional analog circuitry, which suffers from inherent performance limitations and other drawbacks, and the expensive-to-implement building-block DSP components: multipliers, high-speed memories, and support components. Digital-signal-processor consumption, spurred on by the new applications, has resulted in falling prices (Fig. 1), which in turn have heightened interest in finding ever more applications for the product. To many, this situation looks identical to the early days of the microprocessor explosion.

But with microprocessors, system designers asked, "What else can I do with this?" The designers could formulate hardware and software architectures that provided data-processing capabilities not previously available, at least within set cost limitations. On the other hand, designers working with DSP chips usually have to solve problems brought about by the introduction of new technologies—technologies that have increased either the end-user's processing capability or the capacity of a supporting communications link.

One problem is echo cancellation in long-haul voice communications, which can become acute when satellites are used. Another is voice compression for memory-hungry applications such as voice store-and-forward message systems as well as desktop computers with voice recognition capability. For these types of signal processing challenges, designers must ask, "Is this DSP the least painful solution to my problem?"

And the single-chip DSP is indeed finding its market niche. When in place, it provides high performance relative to the board space it occupies, while offering programmability during the product development cycle (see "System designers find answers in digital signal processing," p. 66). Above all, the programmability of these chips opens the door to ever-wider horizons of signal-processing applications.

Without programmability, many new signal-processing applications would call for custom-designed integrated circuits, introducing performance uncertainties and project delays into the development cycle. With a program-



1. Cheaper every day. Production yields are growing as single-chip digital signal processors catch on in more and more products. Increased use leads to price cuts, as is exemplified by the price history of the TMS320 since its introduction in early 1982.

mable chip, however, new products can be developed and tested quickly to meet the needs of changing markets.

Although the driving factors for digital-signal-processor applications are somewhat different from those of the conventional microprocessor, signal-processing developments based on digital-signal-processor chips are following the same well-blazed trail. A successful product relies on the most economical hardware that works, with any performance edge over competing products attributable to the software design.

Technology overlap

Chip marketers, in particular, cannot resist drawing parallels between the DSP and the microprocessor. "What a micro was to logic, a digital signal processor is to analog," proclaims one marketing representative of a digital-signal-processor producer. Not surprisingly, the targeted applications of digital signal processors and logic microprocessors sometimes overlap.

Racal-Vadic, Milpitas, Calif., is introducing a tabletop modem that uses the Intel 8096 in a DSP application. The 8096 handles the 16-point quadrature amplitude modulation for 2,400-b/s full-duplex operation over the switched telephone network.

"The 8096 is really the first microcontroller that can pick up the low-end digital-signal-processor applications," says Robert E. Holm, manager of new product development for Intel Corp.'s microcontroller operation in Chandler, Ariz. Although the 8096's multiply function takes 6.5 μs to complete—it is implemented as a state machine rather than in hardware—Holm notes that the part's unburdened central processing unit helps to open up some applications.

To Philip Goldworth, applications engineer with Fujitsu Microelectronics Inc. in Santa Clara, Calif., a DSP is simply a specialized microprocessor. Goldworth works with the MB8764, the general-purpose, single-chip DSP that is currently the performance leader in terms of the speed in which it executes instructions. Goldworth names high-speed multiplication and quantities of fast random-access memory as two specialized features that distinguish digital signal processors from logic microprocessors, and other experts invariably agree. The threshold multiply speed and minimum quantity of on-board RAM, as well as the multitude of other factors such as input/output characteristics, are usually relative to a digital signal processor's intended function—the algorithm complexity and amount of storage needed for temporary data, results, and coefficients.

The Fujitsu digital signal processor is a CMOS chip in an 88-pin-grid-array package. It executes instructions in 100 ns while dissipating only 300 mW. The internal parallel-pipelined multiplier utilizes a second-order Booth algorithm, generating a 26-bit product from two 16-bit words. On-chip RAM consists of two sets of 128 16-bit words. I/O functions include an on-chip direct-memory-access channel.

Echo cancellation

Because of its high-speed and low-power CMOS design, the Fujitsu part appears to be making some headway into signal processing's most advanced commercial applications. But more important to M/A-COM DCC Inc., Germantown, Md., it is the speed of the MB8764 that virtually mandated its use in prototyping work aimed at adding echo cancellation to the firm's single-channel digital speech interpolator. In its current product configuration—without the echo-cancellation feature—

System designers find answers in digital signal processing

Using digital techniques to process any analog signal requires that the signal first be converted to a series of representative quantized values, or samples. Usually, the digital signal is reconverted to analog form after the processing is complete.

Analog-to-digital and digital-to-analog converters, along with the requisite bandpass filters, take care of the conversions. However, one single-chip signal processor—the 2920 from Intel Corp., Santa Clara, Calif.—is a digital processor that handles signals while they are still in their analog form. Intel's analog signal processor has on-chip ADCs and DACs for the conversion function.

System designers have tended to use high-speed building-block components for performing the multiplications and accumulations that digital-signal-processing algorithms demand. Multipliers, correlators, address generators, memories, and function generators are typically added to the ADC and DAC components when designing a digital signal processor. If the system processing requirements are very high—as in the case of video compression—the performance of individual system components is also pushed to the limit. This high-performance requirement was the motivating factor behind the recent crop of state-of-the-art ADCs that are capable of sampling at the 20-MHz range and above [*ElectronicsWeek,* August 20, 1984, p. 63].

For lower-grade voice and industrial applications, satisfactory building-block components from many suppliers abound, and the trend is towards introducing power-saving CMOS versions of these popular chips. But looming as an even more challenging and economical approach to signal processing are the single-chip DSPs—specialized microcomputers that have shared in the benefits of advanced fabrication processes. These chips contain random-access and read-only memories, multipliers, and accumulators that are implemented in hardware, but are under the control of applications software.

With a digital signal processor assisted by an ADC and DAC and support components such as system clocks, a digital processing system can be configured on a minimum amount of board space. Such a system offers the designer the capability for reprogramming his software, which is virtually a necessity when fitting innovative signal-processing algorithms into a limited number of program steps.

In the case of voice digitizing at the usual 8-KHz sampling rate, 125 μs must be allocated to process one sample before the algorithm can start on the following sample. For a 250-ns DSP, this processing interval corresponds to 500 machine cycles.

the SDSI compresses 96 voice channels into the bandwidth of a single T-1 carrier for either satellite or terrestrial links.

"We needed a digital signal processor that is as fast as the Fujitsu part. For our particular application, a 150-ns digital signal processor would have been too slow," says principle engineer Hyokang Chang. In the speech interpolator, M/A-COM has 256 in.^{2} of board space available for echo cancellation on the 96 voice channels. One chip will be used for each channel.

The echo-cancellation algorithm is proprietary, but according to Chang, it consists of a decision-making part and a number-crunching part. "The processing is dynamically allocated between those two parts," says Chang. The requirements for programmability, processing speed, board space, and power consumption all contributed to the selection of the high-end DSP.

For implementing a new three-dimensional image-synthesis system, Lucasfilm Ltd., San Rafael, Calif., is taking a close look at the Fujitsu DSP. The system is intended for film-production special effects, which requires processing capability on the order of a flight simulator. Systems with this performance usually are implemented with custom hardware.

The Lucasfilm team has ruled out conventional microprocessors and bit-slice parts because these approaches do not offer the performance per square inch needed, according to senior engineer Adam Levinthal. Gate arrays, however, with gate delays in the subnanosecond range, are an option for future generations of the system. Levinthal expects a migration to gate arrays, at least for some parts of the design.

For its image-synthesis system, Lucasfilm selected the Fujitsu part over the other single-chip DSPs primarily because it has excellent I/O characteristics, says Levinthal. On the other hand, he notes that "irregular arithmetic functions" in the architecture might limit the chip's usefulness to the project. "Each of the digital signal processors [that are now available] has different advantages and drawbacks," he explains.

Doubling performance parameters

AT&T Bell Laboratories has used its own DSPs for internal research and development since 1979. The current WE DSP20 contains 256 20-bit words of on-chip RAM and has a 400-ns instruction-execution time—a doubling of the performance parameters of the initial AT&T digital signal processors. The high-resolution 20-by-16-bit multiplier opens the door to speech-processing applications, according to J.R. Boddie, supervisor of the digital-signal-processing group at the Holmdel, N.J., facility.

The DSP20 is also used in AT&T's No. 5 Electronic Switching System. One hundred of these systems, which in sum serve over a million lines, are now in place. The 40-pin n-MOS chips filter out the dial tones from subscribers and also perform line-quality tests.

Hitachi Ltd., Tokyo, has a digital signal processor—the HD61810—that executes instructions in 250 ns. The CMOS chip contains 200 16-bit words of data RAM and 128 words of read-only memory for coefficient storage. Hitachi's part also has a floating-point arithmetic capability (Fig. 2) for the high-accuracy—or wide dynamic range—required in precision speech and telecommunications applications.

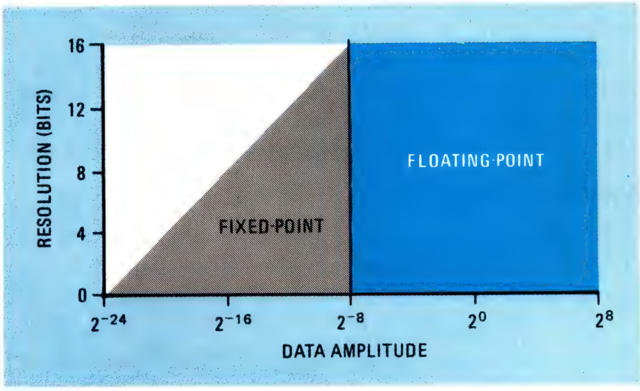
One example of a wide-dynamic-range application is linear predictive coding, a speech-compression technique that yields compression ratios in the 25:1 range. Hitachi reports that a speech-analysis and -synthesis system is feasible with two HD61810s, an 8-bit microcomputer, and support components (Fig. 3). With one DSP performing the spectrum-analysis chore while the other handles pitch detection, the system is a compact solution to implementing linear predictive coding.

Gould AMI Semiconductors' answer to general-purpose digital signal processors is a chip dubbed the Signal-Processing Peripheral. The basic version is the S28211, a 32-pin n-MOS part that features a three-port data memory for its 256 16-bit words of on-chip RAM and 128 16-bit words of on-chip ROM.

Two-word readout

This architecture allows for the simultaneous readout of two data words. For development and low-production usage, the mask-programmable S28211's counterpart is the 64-pin S28212, which has an external instruction memory capability. The S28211/12 executes instructions in 300 ns and contains a 12-by-12-bit multiplier that produces a 16-bit product.

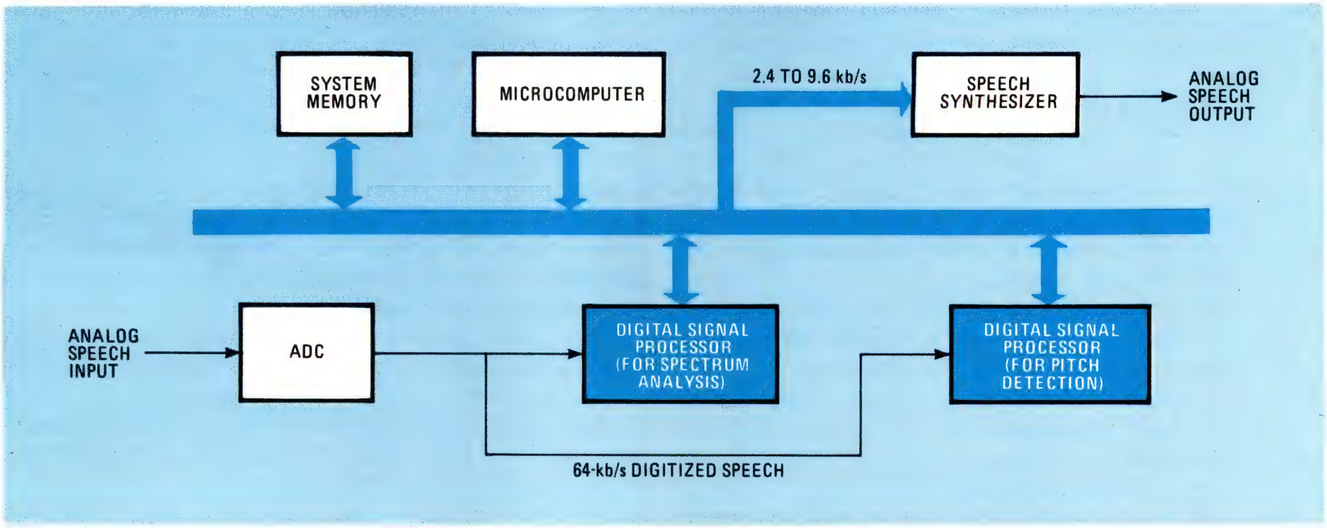
The Santa Clara firm also offers special-purpose parts. "Our strategy is to go after selected areas—high-volume users," says Chuck Kondrath, marketing manager for communications products. The S28214, for example, is a preprogrammed version of the S28211 that performs fast Fourier transforms—a 32 complex-point forward or inverse FFT in 1.3 ms. A decimation-in-frequency technique is employed to minimize distortion.



2. Flexible arithmetic. Hitachi's digital signal processor automatically switches between fixed- and floating-point arithmetic when the data amplitude crosses the 2^{-8} threshold. Thus the chip supports 32 bits of dynamic range as well as a 16-bit maximum resolution.

Besides the routine that performs the 32-point FFT, the program ROM contains five other individual routines, including one that decomposes larger blocks for the 32-point routine to execute. In this way, the chip can handle larger transforms (Fig. 4).

To cover all bases, AMI intends to second-source the NEC 7720. This n-MOS part from NEC has been available from the Tokyo firm for several years. In a 28-pin dual in-line package, its instruction-execution time is 250 ns; besides a multiplier, it provides 128 16-bit words of



3. Compressing speech. For linear predictive coding, one Hitachi digital signal processor uses 131 words of on-chip random-access memory for spectrum analysis. Its companion DSP, however, uses 200 words of RAM—all of the chip's capacity—for pitch detection.

data RAM and 510 13-bit words of coefficient ROM.

General Instrument Corp.'s Microelectronics Division, Hicksville, N.Y., also sees a bright future for single-chip digital signal processors. "Digital signal processing is one of the fastest growing segments of the industry, as an application," says vice president of marketing Ken Greenberg.

General Instrument will second-source the n-MOS TMS320 from the Texas Instruments Semiconductor Group, Dallas. General Instrument is also well along in producing a CMOS version of that popular DSP. The agreement between the two chip houses is that General Instrument, in turn, will transfer the CMOS design to TI for second-source manufacture.

According to Greenberg, goals for the CMOS chip are broader than just a reduction in power dissipation—engineers at General Instrument are shooting for a speed increase, too. Hopes are that samples of the CMOS TMS320 will be ready by March of next year.

Speech coding

TI's n-MOS digital signal processor has an instruction execution time of 200 ns for 90% of its instruction set, and it offers 144 16-bit words of on-chip data RAM. This part finds a wide range of uses. For example, M/A-COM Development Corp. has put four TMS320 digital signal processors together to implement a proprietary speech-coding algorithm. Because the configuration is now in the prototype stage, a capability for reprogramming is essential.

According to Ray Strowh, director of the Signal Processing Laboratory at the firm's research center at Rockville, Md., bit-slice microprocessors would have been the likely choice of technology had the single-chip DSPs not been so readily available. For future versions of the product, "the entire coder might be built with two Fujitsu chips plus board parts," says Strowh.

Another company that passed over bit-slice parts in favor of the TMS320 is Votan, Fremont, Calif., which was able to replace four Am2901 bit-slice microprocessors with one digital signal processor for its current line of voice-recognition and message store-and-forward products. The card-level solutions rely on proprietary algorithms for continuous speaker-dependent recognition and compression. Recognition response time is under a half second for a vocabulary of 150 double-trained words. The compression algorithm achieves toll-quality performance at 10 kb/s.

In West Germany, ITT Intermetall GmbH, Freiburg, has in the works a monolithic digital signal processor. Shown this month at the Electronica exhibition in Munich, the 2.4-μm CMOS chip is called the UDPI—for Universal Digital Processor, Industrial. Its pipelined Harvard structure supports instruction execution times between 100 and 300 ns. Power dissipation is 500 mW.

On-chip features include a 16-by-16-bit parallel multiplier that produces a 31-bit product in 200 ns, 440 16-bit words of data RAM, 72 words of data ROM, and 1,000 words of program ROM. In development is an emulator chip with an external program bus for hooking to program ROMs.

ITT Intermetall expects the UDPI to find work across the broad spectrum of applications including filtering, speech synthesis and analysis, FFTs, and equalizers. The company further projects that DSP chips will account for 15% of its total sales in 1985.

Ultra-high-performance applications

Other IC suppliers intend to add single-chip digital signal processors to their product lines. Not the least conspicuous of these companies are the ones that are now industry leaders in ultra-high-performance building-block components. Military systems, diagnostic instruments for the medical profession, seismic analysis, and weather forecasting are all traditional applications for building-block components, and demand in these areas is expected to remain high. Yet some of these chip vendors are looking to single-chip digital signal processors, and for good reason.

"A lot of our customers are looking at the single-chip solutions," says Frank L. Toth, marketing manager for the Digital Signal Processing Division of Integrated Device Technology Inc., Santa Clara. The firm specializes in a CMOS product line of building-block digital-signal-processor components, including a 16-by-16-bit multiplier with a 65-ns worst-case clocked multiplication time at 220 mW of power consumption. Integrated Device Technology plans to introduce a single-chip digital signal processor, perhaps in 1985.

LSI solutions

In the process of expanding its DSP product line into CMOS is TRW Inc.'s LSI Products Division, La Jolla, Calif. "Today the digital products need to be CMOS," says Darrell Mayeux, director of sales and marketing. One of TRW's newest CMOS parts is the TMC2009, a 12-by-12-bit multiplier-accumulator that is pin- and function-compatible with the company's bipolar TDC1009. But the CMOS part operates at the same speed, 7.4 MHz, and consumes only 200 mW of power, less than one fifth that of the bipolar version.

TRW also plans to jump into the single-chip digital-signal-processor market, with introductions beginning in 1985. The firm will concentrate, Mayeux says, on optimizing the architecture of each digital signal processor for a specific application; he indicates that the parts will be cast in CMOS and will provide an instruction rate of at least 10 MHz.

Another firm active in high-end building-block components is Weitek Corp., Sunnyvale, Calif. According to vice president for technology Chi-Shin Wang, Weitek will continue to concentrate on the high-end DSP market, paying particular attention to solids modeling in graphics. Recently, Weitek added CMOS parts to its 16-by-16-bit multiplier and multiplier-accumulator line, and reports that these new TRW-compatible parts dissipate 75% to 80% less power than their n-MOS predecessors, while operating at least 25% faster.

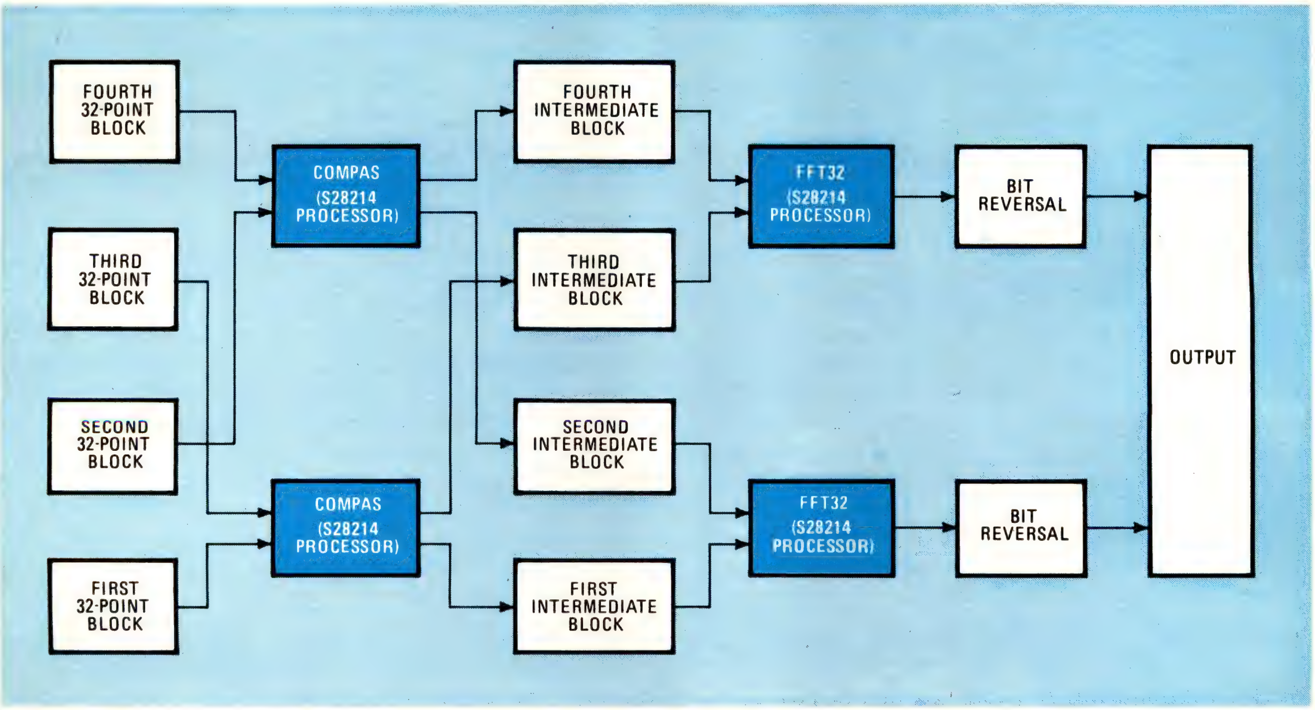
Advanced Micro Devices Inc., Sunnyvale, has employed its IMOX-S process [*Electronics*, June 28, 1984, p. 131] to speed up its 16-by-16-bit multipliers. The 29516A/29517A multipliers offer a better than 40% speed improvement over the 29516/29517—typical clocked multiply times for the IMOX-S chips hit 30 ns. As a lower-power option the 29L516/29L517 parts multiply in the 70-ns region while dissipating 1.5 W. Future plans are to introduce CMOS versions of the multipliers.

Analog Devices, Norwood, Mass., is another leader in high-performance building-block components. By the end of 1984, the firm expects to have in production enhanced versions of its CMOS multipliers and multiplier-accumulators. The ADSP-1016A executes a 16-by-16-bit multiplication in 65 ns, which more than doubles the speed of the 1016.

The part's 64-pin DIP allows for two 16-bit input buses and one dedicated 16-bit output bus—one of the ports handles the least-significant output word. Another three-port chip, the ADSP-1024, executes a 24-by-24-bit multiplication in 175 ns. This is the industry's first 24-bit multiplier, according to digital-signal-processor marketing manager Ted Dintersmith.

The Analog Devices ADSP-1008A performs its 8-by-8-bit multiply and accumulate operation in 45 ns—compared with 105 ns for the 1008—and the 16-by-16-bit 1010A multiplier-accumulator will multiply in 65 ns, an improvement by almost two thirds over the 1010's 165 ns. Another new introduction, the ADSP-1110, is a single-port multiplier-accumulator being offered in a 28-pin DIP. It accomplishes a 16-by-16-bit multiply and accumulate task in 190 ns. Dintersmith indicates that this part is the headliner among his new DSP components. "It's still a fast digital signal processor part, but it takes up less board space." ☐

John Gosch, in Frankfurt, West Germany, was a contributor to this special report.



4. Building FFTs. For 64-point fast Fourier transforms, the S28214's preprogrammed routines can be carried out sequentially or in parallel, using two digital signal processors. The Compas routine decimates the input into two 32-point transforms, which the FFT32 routine executes.

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FLEXX ARRAYS SPEED IC DESIGN

New semicustom technique combines best features of standard cells and gate arrays in powerful, easy-to-use approach

☐ *by Bill Loftis and Herb Jesse*

Claims and counterclaims from suppliers of gate arrays and standard cells are unending. Regardless of the method used, whether gate array or standard cell, it seems clear that the choice of a semicustom approach to a given project offers both drawbacks and advantages. Since initial favorable impressions will be short-lived if performance doesn't measure up, it is apparent that the perfect solution has yet to emerge.

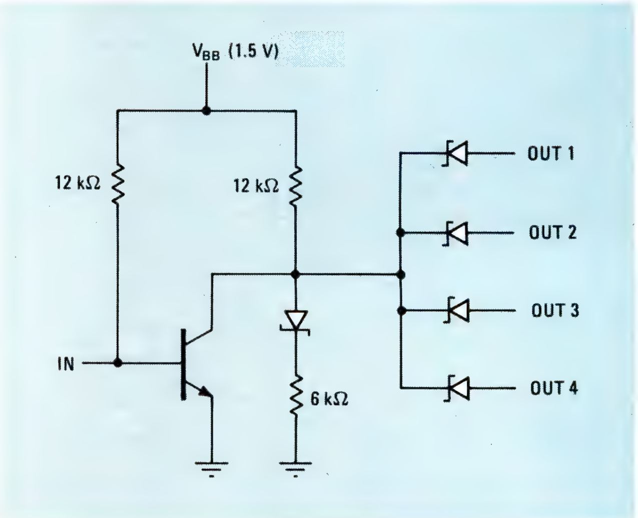
The Flexx array approach to the design of integrated circuits preserves the advantages of both gate arrays and standard cells, while at the same time eliminating the drawbacks. Several features set the Flexx array apart:

- It is completely automated. The design work station can be either an IBM Corp. Personal Computer XT with FutureNet Dash-1 or a Mentor desktop work station.
- Where a gate array—sometimes called a sea of gates—wastes silicon because it's not possible to use all the gates and input/output devices in most designs, the Flexx array is completely silicon-efficient, because only the required gates and I/O devices for a particular application are implemented.
- Routing inefficiencies in gate arrays, caused by routing-channel limitations and shortcomings in place-and-route programs, add significantly to signal-propagation delays. The Flexx array eliminates this problem with a design that is 100% autorouted and employs both a fixed grid and a variable channel router, which results not only in minimization of die size, but also optimizes critical paths.
- Using standard cells, the designer must pick logic functions from a fixed library of hard macrocells. Inevitably, a great deal of logic within a macrocell goes unused because the application requires a simpler macrocell that is not available in a given library. With the Flexx array, a new concept that uses soft macrocells has been created, allowing either the elimination of unnecessary gates or the addition of new gates. Also, completely new macrocells can be rapidly created for repeated use. A Flexx array thus offers not only a variable die size but also no unused circuitry.
- The Flexx array concept is technology independent. That is to say, it is able to implement the desired circuit in different types of technologies. At the present time, arrays in integrated Schottky logic (ISL) bipolar technology are available, and CMOS will be available in the very near future.

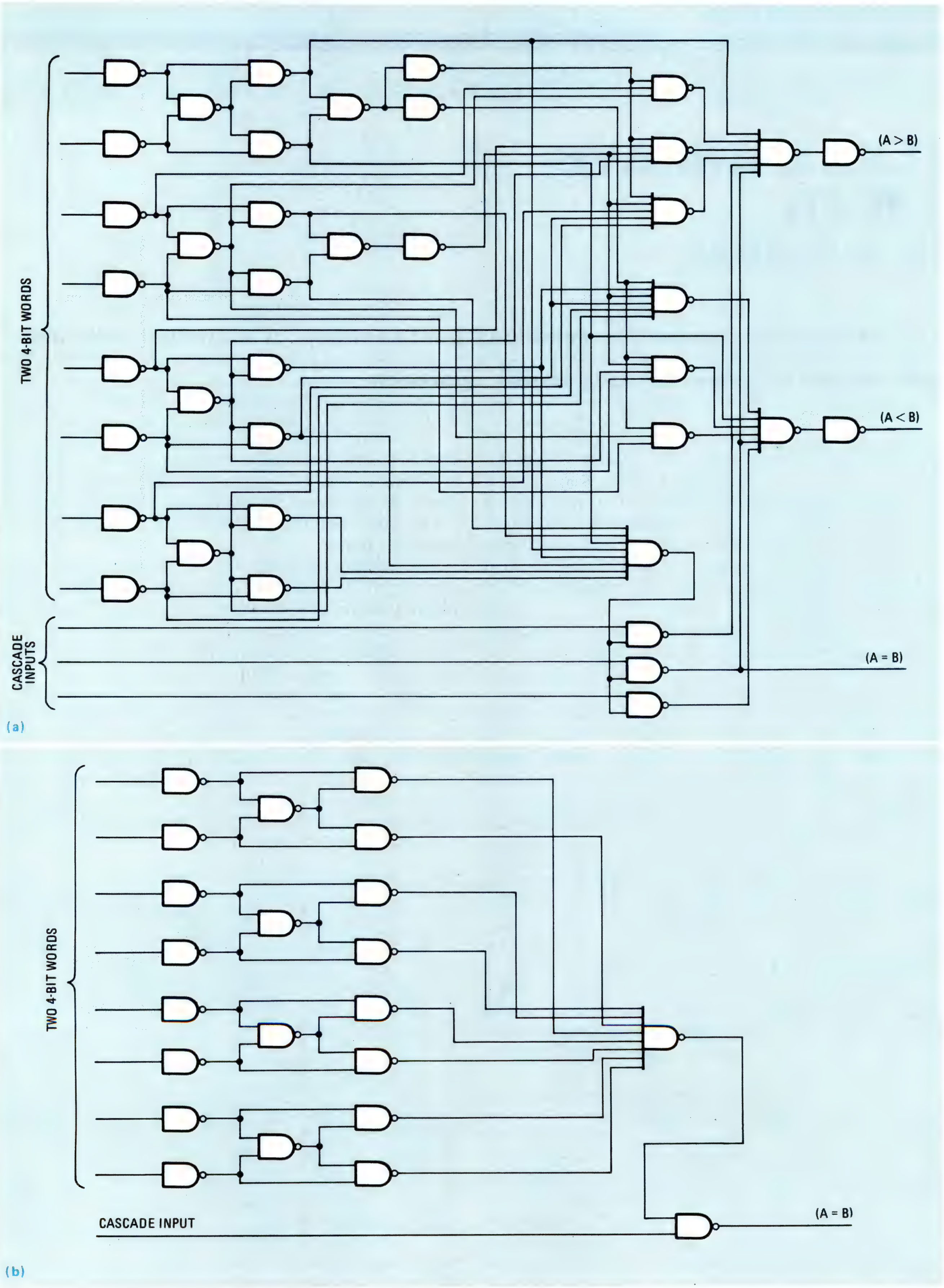
This technology independence extends to the extensive set of user-friendly computer-aided design tools which have been developed to support the concept. The same tools permit designs in both bipolar and CMOS across a broad speed range—from subnanosecond logic to very low-power CMOS.

Finally, when a complete circuit designed as a Flexx array is compared with the same circuit in any other semicustom technique (given comparable design rules), the Flexx array die is usually significantly smaller.

An oxide-isolated ISL gate (Fig. 1) is offered in the current version of the Flexx array. Its speed capability (900 ps) and high drive (up to 100 mA) places resulting products squarely in the mainstream marketplace. Fur-



1. Flexx gate. An advanced oxide-isolated integrated Schottky logic (ISL) bipolar NAND gate provides the basic gate element for the Flexx array soft-macrocell structure. It operates in less than 900 ps, and has a drive capability of up to 100 mA.



2. Flexxing your macro. A full 74LS85 magnitude comparator (a) with A = B, A < B, and A > B functions implemented. If only one function is desired, the gates for the others are unused. In the Flexx macrocell (b), the gates associated with the undesired functions have been deleted.

thermore, the ISL NAND gate represents significant engineering experience and offers continued performance improvements through process upgrades.

Traditional standard-cell approaches, such as Signetics Corp.'s Composite Cell Logic, are die-size efficient because only the cells used are placed on the chip. But the effort to develop a complete library (80 or more cells) can take many man-years. For this reason, standard-cell libraries are typically a generation behind the latest process technology.

Variable ponds of variable gates

On the other hand, gate arrays are relatively simple to design because there is usually only one basic internal gate replicated into a sea of gates, plus a handful of different I/O structures. Often, therefore, gate arrays offer advanced process technology and design rules. From a user standpoint, they are a more difficult design medium because of their more primitive internal gate structure (usually NAND or NOR).

With classic standard cells, primitive gates are combined with higher-level logic functions (flip-flops up to the medium-scale integration level). To the engineer, the logic-design task is simplified by permitting design at a higher level; the user need not worry about how to build a D flip-flop using NAND or NOR gates, assuming of course that all higher functions have already been laid out into characterized, documented hard macrocells.

By contrast, the Flexx array combines the best qualities of both the standard cell and the sea of gates. As with gate arrays, the internal cells are few, allowing the use of the latest oxide-isolated technology. As with standard cells, the design methodology is macrocell-based and die size is variable, depending only on the number of macrocells and/or gates used in the design. If each Flexx array macrocell is thought of as a pond of gates, the user begins to sense that the Flexx array is an array of arrays.

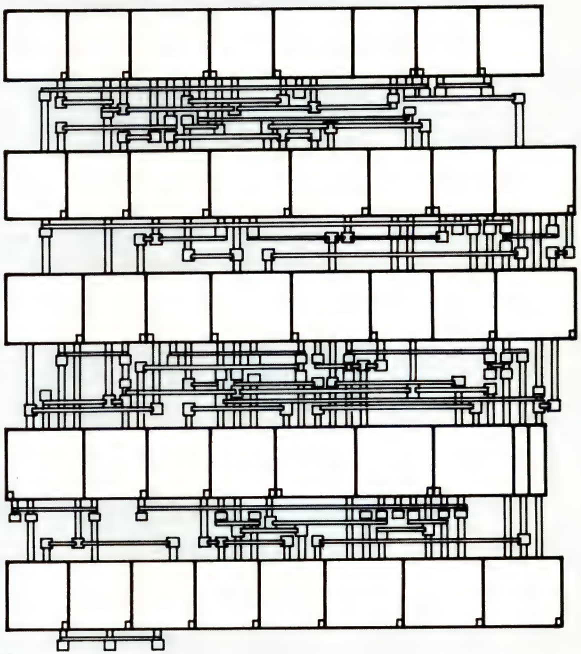
Soft macrocells

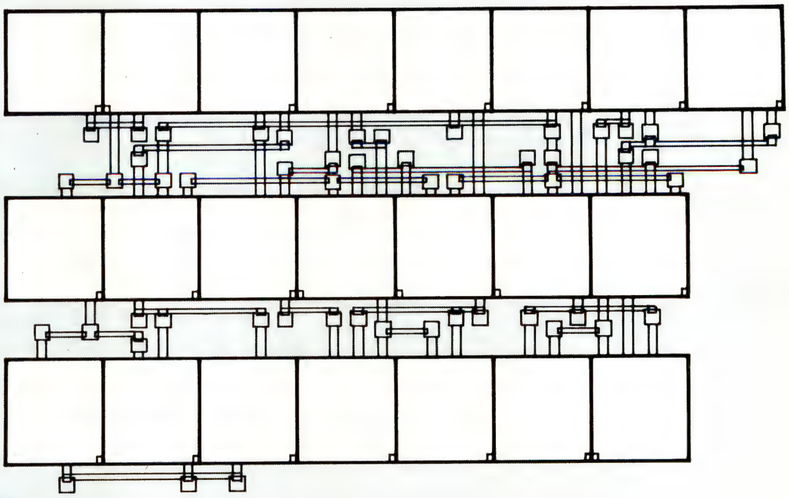
The Flexx array is supported by both proprietary and commercially available software so that the user can implement logic at any desired logic level through the use of soft macrocells. These soft macrocells are developed from the primitive internal gate into higher and higher levels of hierarchy. Unlike hard macrocells, the soft macrocell is not already laid out, nor is it geometrically fixed in orientation with rigid metalization and I/O requirements. The layout task is relegated to powerful software where silicon efficiency is manifest.

A library of basic soft macrocells is offered to the user, as in any standard-cell approach. The user can select any macrocell and use it as is. Alternately, the user can easily and directly modify a macrocell or create an entirely new macrocell without losing the soft characteristics.

Several dozen soft macrocells have been developed and debugged for the Flexx array, with new macrocells coming weekly. The development involves creating a graphic representation and then simulating the macrocells (as though they are a complete circuit) to verify functionality and characterize typical delays. Because they constitute the most homogeneous and widely accepted circuit form, standard 7400-series TTL functions are used in the basic Flexx array repertoire. They use industry-standard names to easily select new designs and replace existing designs based on 7400-series logic. The nearest 7400 equivalent may contain a dual, quad, or octal combination of the same gate or function; however, the Flexx array macrocell contains only a single gate or function. This feature allows placement of gates or functions at optimum locations. All macrocells, whether hard

3. Real estate. The layout in silicon for the 74LS85 shown in Fig. 2 (a) before modification by Flexx array, and (b) after the unused gates have been removed. The Flexx array layout actually is about one half the size of the unmodified layout.





or soft, are easy to work with, especially when upgrading an existing design based on 7400 TTL.

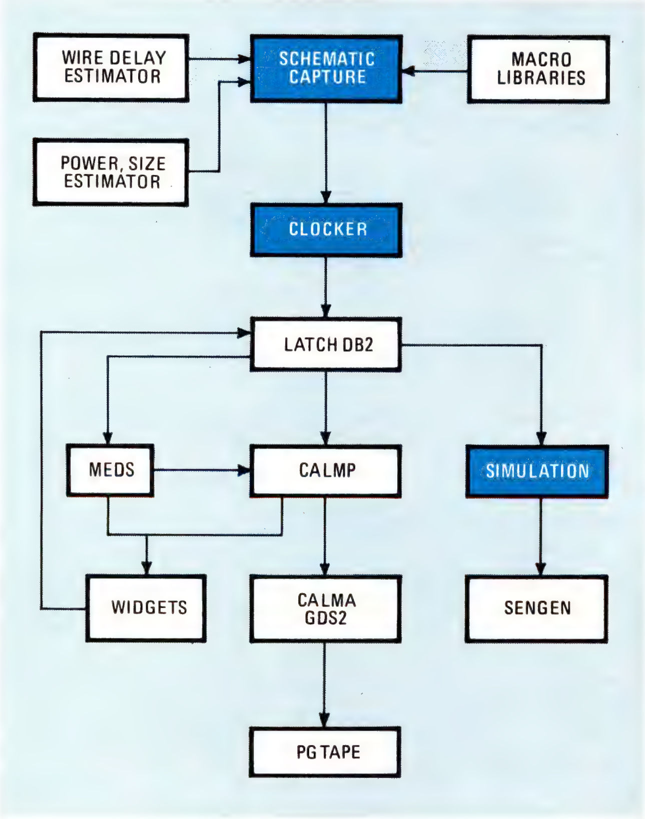
Macrocell selection is a trivial exercise. When the same exercise is considered by the integrated-circuit designer (rather than the logic designer), standard-cell macrocells fail the test of silicon efficiency. For example, in a design that uses the 74190 up/down counter in an application requiring only an up-counter function, the unused gates in the macrocell have a detrimental effect on speed, power, and die size. If the full cell design employs many similar functions, the final cell wastes a considerable amount of silicon.

The dramatic savings inherent in soft macrocells is easily illustrated. The soft macrocell for a 74LS85 magnitude comparator (Fig. 2a) requires 39 internal gates. If, in the actual application, only the A=B output is required, the macrocell could be reduced to only 22 gates (Fig. 2b), a significant 44% reduction in gate count.

Soft is better

The user's ability to modify existing macrocells is the real strength of the Flexx array concept. The real estate used for the 74LS85 after modification (figures 3a and 3b) is 52% smaller. On all performance counts—real estate, gate count, and power consumption—this typically means more than a 50% improvement.

The logic inefficiency at the boundary of these macrocells, which is caused by the need to maintain all logic levels as active high, is also improved. In logic design, there are many cases in which the output of a flip-flop can be taken from $\overline{Q}$ rather than Q, thus eliminating a gate in the next stage. The Flexx array offers both choices: modifying or creating a unique macrocell to fit the exact need, or using the macrocell as is.



4. Flexx flow. An input flow chart shows the software sequence that totally automates the process of Flexx array design, beginning with schematic capture and ending with a pattern-generation tape. Highlighted areas denote customer's responsibilities.

Modifying soft macrocells is straightforward and foolproof. Each macrocell data sheet includes typical delays (final delays won't be known until layout is complete) and graphics detailing internal connections. Because of the CAD tools, the user can call up this graphic macrocell and modify and save it under a new name. The new macrocell is then simulated for functionality and timing to immediately reveal hook-up or logic errors.

Puny penalty, big benefit

For a given fixed function, a hard, precharacterized standard-cell macrocell will always be laid out more efficiently than a soft macrocell. The hard macrocell has been popular for some time because worst-case propagation delays are well known and can be fully simulated and verified by way of characterization. However, hard macrocells are not efficient in the global sense because they are physically larger puzzle-pieces that must be made to fit into the chip according to strict design rules. Also, hard macrocells have predescribed logic inefficiencies firmly locked in.

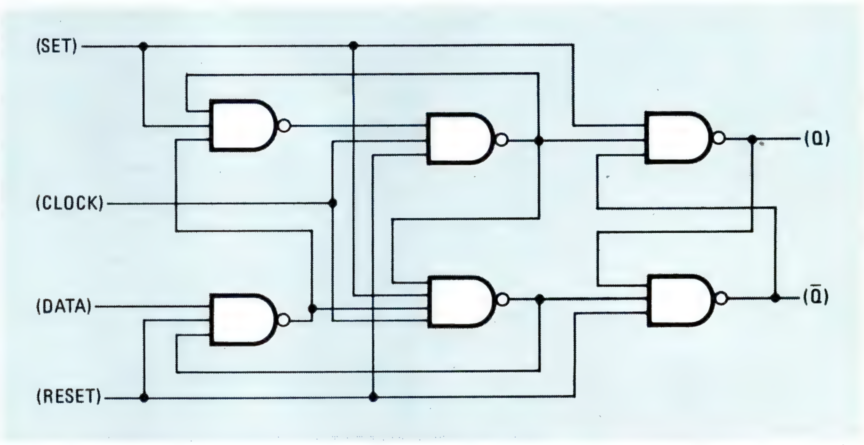
With the Flexx array, this problem is solved by accepting a small area penalty in exchange for a lot of design freedom. To demonstrate this, a D flip-flop was laid out first as a hard macrocell, then as a Flexx array macrocell under the concept of dividing a soft macrocell into NAND gates. A comparison of the two sizes showed that there was a 12% area penalty for the Flexx array. However, though the hard macrocell is somewhat smaller, it completely lacks the flexibility to be tailored to the application.

Yet even the area penalty can be recovered, if a user-modified macrocell that is critical to a specific application is saved in the physical layout for future use. This capability is manifest in the CAD tools that support the Flexx array—notably the Meds automatic place-and-route program developed by Scientific Calculations Inc., Fishers, N.Y. For example, at times every flip-flop has to perform in exactly the same manner; a hard layout is required to ensure uniformity.

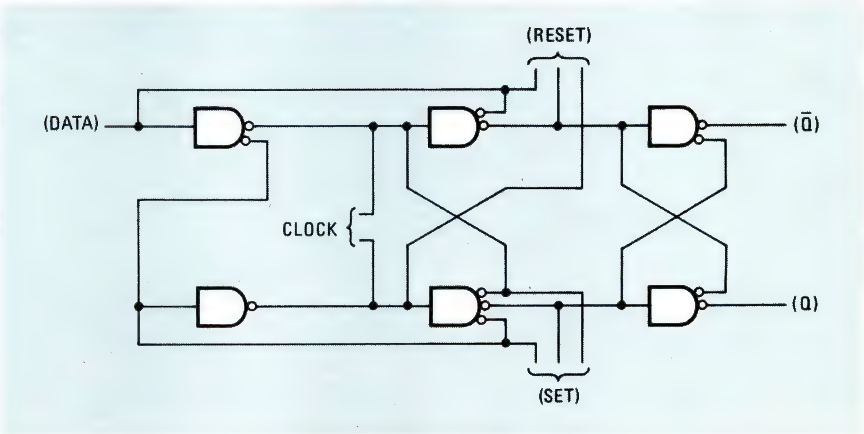
Getting the Flexx array's benefits in practical array design means that the desired logic will be flattened or decomposed from the top level of the hierarchy all the way to the bottom level prior to routing. If the design is stopped part way down the hierarchy to build flip-flops, which are then used to build a counter, each flip-flop has a small area penalty that is multiplied by the number used. Because the flexibility gained far offsets the area penalty, resulting in a final design that approaches hand-packed density, the Flexx array cell is an obvious improvement.

By the same token, there are times when chip architecture is very regular; saving some or all of the macrocell layouts may result in greater overall efficiency. The Flexx array allows this when needed.

Not-so-obvious advantages of saving layouts also come from the CAD tools that support the Flexx array. For example, the Meds program will automatically route within the boundary of a cell. As a result, a Flexx array flip-flop uses 7.3% less real estate than achieved with a macrocell routed only with CAL-MP, developed by Silvar-Lisco, Menlo Park, Calif. Furthermore, it is only 4% larger than a hand layout. This significant saving returns most of the area penalty suffered by using soft macrocells. The hand layout took approximately 12 calendar weeks and several people to design; the Flexx array macrocell took less than 1 minute.



5. Soft macrocell. A soft macrocell for a D flip-flop before modification to a Flexx array is at the most primitive level. This is the basis for operation by the Flexx system in order to transform the primitive gate layout to a Flexx array.



6. Transformation. The primitive-level soft macrocell shown in Fig. 5 is transformed to the actual internal primitive integrated Schottky logic gates that are used in the Flexx array. The performance of this step is transparent to the user.

Designers who want to reuse high-level macrocell definitions with different process technologies will appreciate an additional benefit of this feature: with the Flexx array, the primitive gates at the lowest level can be replaced. A design for one process technology, with its specific speed and power characteristics, can be converted to a different technology by resimulating it with appropriate models.

Logic compilation

The Flexx array compiles logic according to the classic formula: powerful software tools that allow the user to operate at any level of the design hierarchy transform the logic drawn on the engineering work-station screen into an IC layout (manufacturing tooling). In a process that can operate invisibly to the user, what is drawn is converted to the best choice of primitive gates.

This turnkey, process-independent approach never requires the user to perform circuit-level simulation (Spice, for example). CAD-managed simulations are performed at the logic level and include parasitic capacitance effects on propagation delay. (Experience has shown that users of semicustom logic do not want to use transistor-level simulators, because the complexity only adds to the risk and throughput time.)

The physical detail of Flexx array circuitry is completely abstracted into higher-level modules; electrical and spatial design rules are inherent in the software, which uses a graphic structural approach to compile down to a textual netlist and functional description of the primitives. The point is to optimize layout and logic from the primitive level upwards.

Using the Flexx array concept

Design of a new array begins with schematic capture. For designers equipped with an IBM Personal Computer XT with the FutureNet Dash-1 system installed, a set of floppy disks and training manuals is supplied. A training class is given to familiarize the user with Flexx array libraries and the custom operating software that performs rule checking and some of the compilations. The schematic is entered through the work station.

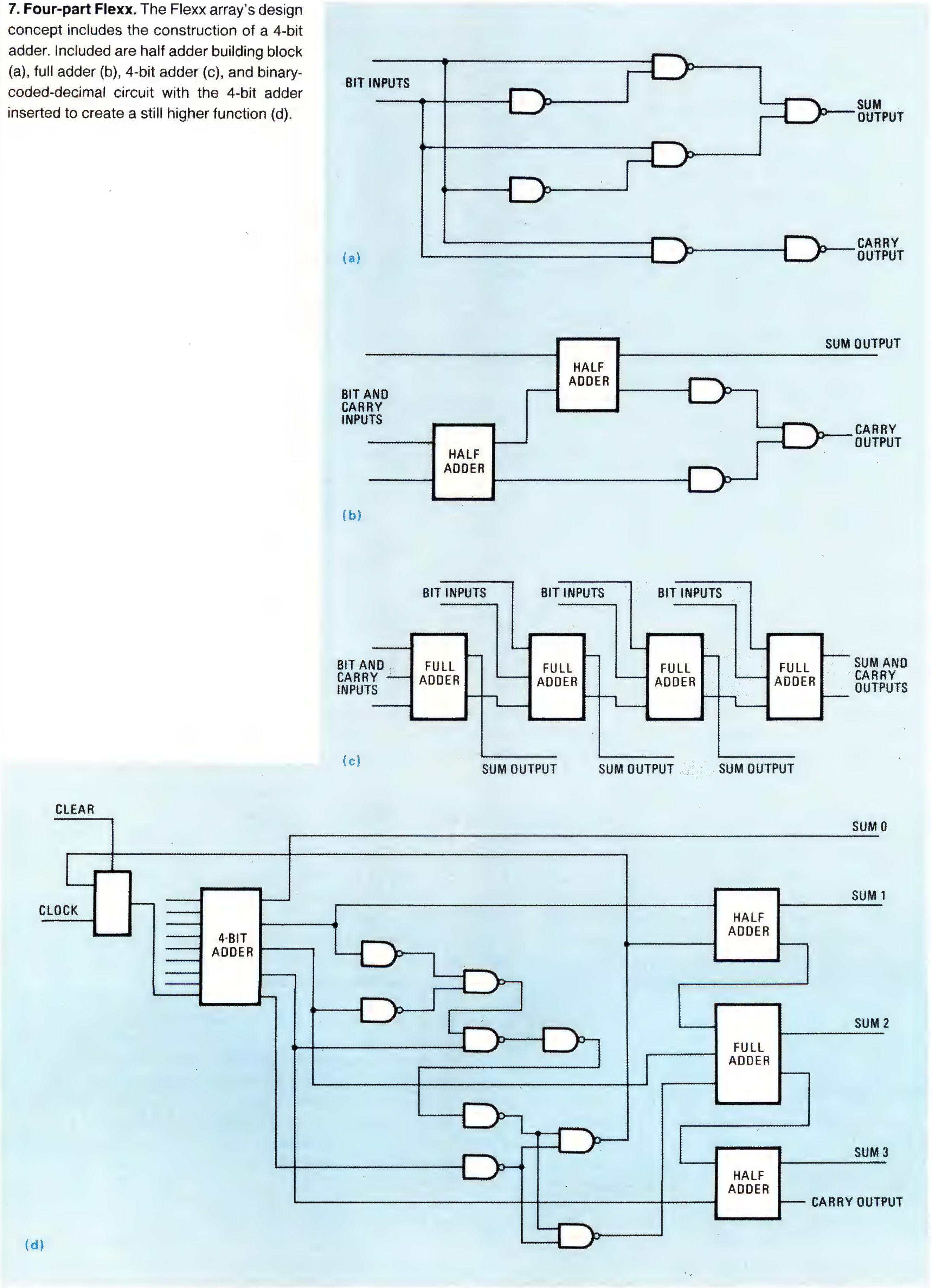
Logic simulation and timing verification are then performed through a modem link between the work station and an IBM 3081 mainframe at Signetics, using a Tegas 5 logic simulator. File transfers as well as timeshifted transfers of large files, without the intervention of the designer, are handled by the system software.

The PC XT automatically dials the host, transfers the necessary input files for simulation and redials periodically while the output is being finished. When simulation is complete, the files are transferred back to the PC XT hard disk for examination by the designer.

For designers with a Mentor Graphics work station, a set of floppy disks with library information and operating software is provided. The user here also begins with schematic capture, but all logic and timing verification is performed using the Mentor simulator at the designer's facility. Other popular work stations—Daisy and Valid, among them—will be included in the future.

The user's schematic input for a Flexx array is through menu selection of the logic macrocells. The system is totally hierarchical in its ability to do top-down designs from the high-level macrocells (Fig. 4). Collapsing the macrocells into the core cells is totally automatic with the supplied software. The transformation, prior to simulation and layout, to convert the more user-friendly multiple-input/single-output gates to the actual ISL sin-

7. Four-part Flexx. The Flexx array's design concept includes the construction of a 4-bit adder. Included are half adder building block (a), full adder (b), 4-bit adder (c), and binary-coded-decimal circuit with the 4-bit adder inserted to create a still higher function (d).



gle-input/multiple-output gates on the current Flexx array product is invisible to the user (Figs. 5 and 6).

An error-checking program (Clocker) detects logic-rule violations (illegal cell types, fan-in or fan-out violations, illegal connections, and so forth). A unique proprietary wire estimator program is then exercised to estimate added wire delays based on fan-out and the priority assigned to the wire by the customer. Another CAD program evaluates how logic changes will affect the estimated die size and power of the final chip. The user is advised on the work station, so that problems can be avoided before layout.

The final, correctly simulated circuit will be automatically placed and routed using a combination of the commercially available CAL-MP and Meds routers. Absolutely no floor planning is required. Another program calculates the power and ground metal widths necessary for both voltage-drop and current-density considerations.

Scribelines, alignment marks, and layer identification are all that remain to be added after routing to create a pattern-generator tape. Proprietary software that drives a Calma adds these features automatically.

In creating a 4-bit adder macrocell, the use of the Flexx array design concept is illustrated (Fig. 7). At the beginning of the process, customers have the option of using one of Signetics' existing soft macrocells or of building their own; the latter offers several paths. Customers can use only primitives (NAND gates) or combinations of primitives and either Signetics' soft macrocells or their own previously created soft macrocells. One of the easiest ways to create custom macrocells is to pull an existing macrocell from the library, modify it by adding or removing gates and wires, and then save it on the disk, using a new name.

The gates for a half-adder (Fig. 7a) make up the building block for creating the final macrocell. This is accomplished by pulling the primitive gates (AGISL1 and AGISL2) from the supplied library and interconnecting them as needed. Before proceeding, the macrocell should be checked for logic-rule and fan-out violations using a supplied program (Teglock).

The second step is to create a symbol for the half adder that describes the number and names of each signal entering and leaving this block. By including in the symbol's name the same name as on the associated logic diagram, the two descriptions are linked. This symbol is then placed in the full adder circuit (Fig. 7b) and interconnected to form the full adder. Again, this level of the hierarchy must be checked with Teglock before proceeding to a higher level.

Levels of hierarchy

A symbol is now created for the full adder, and this symbol is placed and interconnected to form a 4-bit adder (Fig. 7c). After running Teglock, the user could define this as a symbol and place the macrocell in a still higher function, such as a binary-coded-decimal circuit (Fig. 7d). During the creation of these levels of hierarchy, it is recommended that the customer simulate each block as it is developed, since it is easier to debug small circuits than complex ones.

After routing is complete, it is necessary to resimulate the network with the actual values of the metal-interconnection delays added. A Signetics-developed program (Widgets) automatically calculates the value per wire and generates an updated simulation model. This opens up an important virtue: at the schematic-capture phase, the user can set critical-path priority on certain nets that must have minimal delay. If overused, however, this feature may result in a die size penalty because of constraints during routing. It is generally best to proceed all the way through the first layout, and then use the results to decide where priorities return the greatest benefit.

The role of CAD

Test programs are automatically developed using Sengen, which extracts test vectors from the simulation file and generates a Sentry-compatible test tape. Dc parametric information is predetermined by the type of I/O cell selected and requires no hand editing.

Dynamic measurements on the first wafers (oxide-isolated ISL) have shown that the typical gate delay at room temperature is 900 ps, while drawing only 245 μW. Using these numbers as a guide, along with physical die size versus package limitations, it is possible to implement blocks of logic as large as 2,000 gates and to support toggle frequencies of 100 MHz.

With the Flexx array, there is no worry about routability: the concern of partitioning logic to fit onto a specific array is eliminated. Because there are no limitations on the number of I/O buffers available, the concern is only with how many pins are available for the package under consideration. Signetics I/O cells offer current-handling capabilities of 8, 16, 24, 48, and 100 mA.

To prevent a designer from creating a circuit that will not fit into a specific package or that exceeds the package's thermal considerations, a program exists as part of the schematic capture that gives the designer an estimate of the die size and power consumption of the circuit being designed.

Since the Flexx array technique results in a die that does not exceed size, power, and I/O limitations, the resulting part can be assembled into any standard dual in-line package or chip carrier up to 84 pins. Pin grid arrays in the popular 128- and 144-pin packages will be available in the near future.

As the designer has the hardware to do the schematic capture and simulation, the development cost to take a design from a completed simulation file to 50 fully tested prototypes is $20,000 to $30,000. The development time is in the order of 12 to 14 weeks.

Since the die size, package, and manufacturing volume all are variables, the unit cost of a Flexx array can range from $1 to $20 per unit for commercially processed chips. Once a code is developed and deemed functional by the customer, screening to MIL-STD-883B will be offered by Signetics.

A CMOS version of the Flexx array is in development, and in addition an ECL version is being prepared. The Flexx array's design flexibility will also be augmented by offering on-board, user-configurable random-access and read-only memory. ☐

Bill Loftis is an engineering manager and Herb Jesse is the Flexx array product marketing manager at the LSI Division, Signetics Corp., Sunnyvale, Calif.

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CIRCUITS PROVIDE CHEAP VOLTAGE PROTECTION

Three-terminal or pin-programmable overvoltage-sensing circuits join with a few other circuits to provide crowbar protection

□ *by Steve Zollo*

Usually, a customer pays extra for a power supply with overvoltage-protection circuitry. But now, thanks to a pair of inexpensive overvoltage-protection circuits from Motorola Semiconductors Inc., that circuitry will be cheaper to integrate or buy.

The three-terminal overvoltage-sensing crowbar circuits, in models MC34061 or MC34061A, combine with two external programming resistors and a crowbar silicon controlled rectifier to protect sensitive electronic circuitry from overvoltage damage. The parts sense an overvoltage condition and quickly crowbar—or short circuit—the supply.

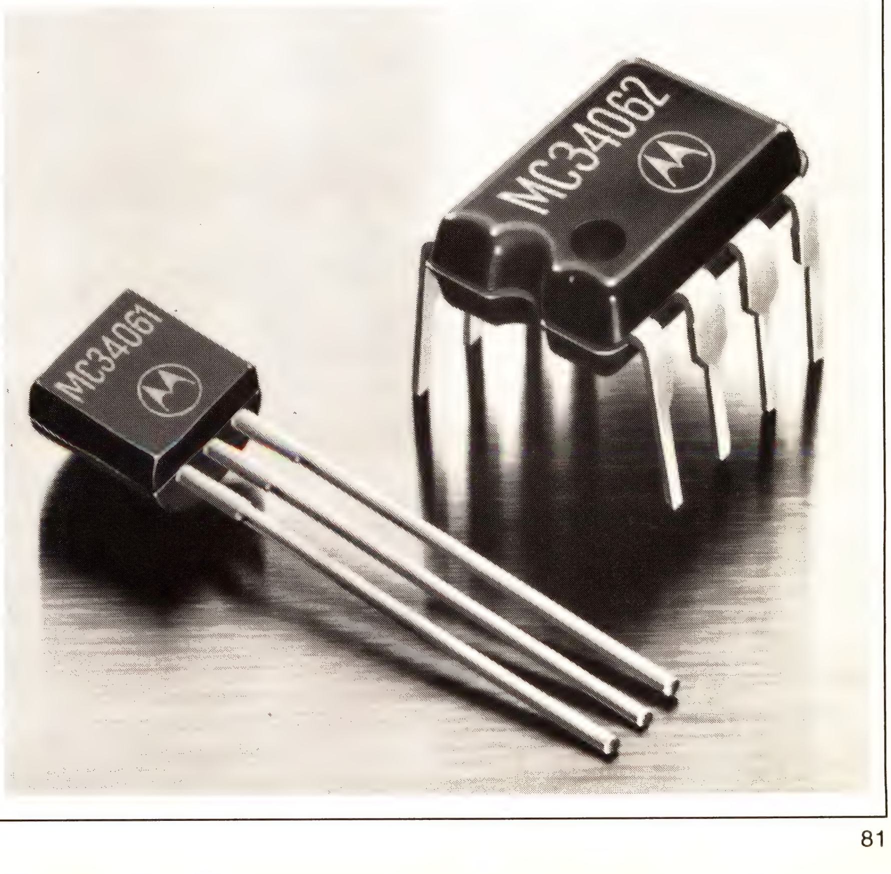
The basic 34061 circuits offer a ±2% tolerance on the sense trip voltage. The A-suffix pieces have a ±1% sense-trip-voltage specification, and other key parameters have tightened limits. Hysteresis is specified at 250 mV. In an 8-pin plastic dual in-line package and a specified operating range from 0°C to 70°C, the parts sell for 65¢ each in lots of 100 to 999. A part in a TO-92 package is also available, as is a military-temperature-grade part, model 35061.

For power supplies above 11 V, a gate resistor in series with the SCR gate is recommended to limit the power dissipated by the circuit to approximately 2 W. This resistor protects the 34061 in the event of a defective or missing SCR, while allowing the maximum drive-output current to the SCR's gate. By simply adding an external capacitor, a time delay may be programmed into the circuit's operation to provide for noise immunity.

The second circuit, the 34062, is a pin-programmable crowbar circuit and requires only an external SCR to work. An on-chip tapped resistor network allows the circuit to be programmed for trip voltages ranging from 3.5 to 40 V. Each of the five programming pins provides one standard overvoltage trip point for normal power-supply voltages of 5, 12, 15, 24, or 28 V.

Other trip voltages may be programmed by interconnecting and grounding various combinations of these programming pins. As with the 34061, the addition of a capacitor allows for the programming of a time delay to provide noise immunity; again, a gate resistor is advised for power supplies above 11 V.

Available only in an 8-pin DIP, the 34062 sells for 75¢ each in lots of 100 to 999 pieces. Delivery is from stock but may take up to six weeks. The military-temperature-grade 35062 is also available. The company is currently



working on surface-mountable versions of both circuits.

Motorola Inc., Semiconductor Products Sector, P.O. Box 20912, Phoenix, Ariz. 85036. Phone (602) 897-3840

[Circle reader service number 338]

Digital oscilloscope performs 200-MHz sampling, analysis

A dual-channel digital oscilloscope and waveform analyzer, the model NIC-320, has a bandwidth in excess of 25 MHz and input voltage ranges of ±150 mV to ±60 V, full scale. Each input incorporates a 10-MHz, 8-bit digitizer for fast transient measurements combined with a sampling mode of up to 200 MHz for studying repetitive signals.

Up to 100% full-screen pretrigger information and a 10-s post-trigger delay can be selected. With the instrument's two 4,000-point memories per input, newly acquired waveforms can be compared with stored data. An annotated display helps improve signal analysis.

Once stored, signals can be manipulated with a variety of mathematical functions selected from a menu through a two-button sequence. For automatic and repeatable sequences, programs can be linked. If further analysis is required, waveforms can be transmitted to other computers over an RS-232-C or IEEE-488 interface. An optional 1-Mb magnetic bubble memory can store up to 21 4-K waveforms indefinitely.

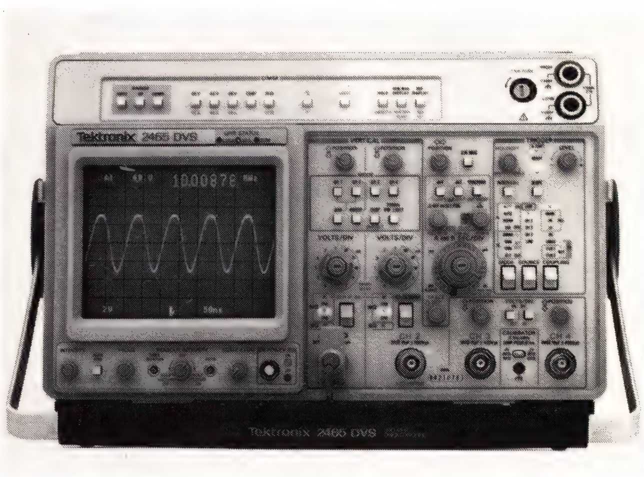
Priced at $7,900, the NIC-320 can be delivered within 120 days.

Nicolet Instrument Corp., Oscilloscope Division, 5225 Verona Rd., Madison, Wis. 53711. Phone (608) 273-5008 [Circle 358]

2465-based oscilloscopes target vertical applications

Three enhanced oscilloscopes are based on the 300-MHz portable model 2465. The packages, called the 2465 Special Editions, simplify measurements and extend capabilities for a range of applications. They operate as standalone units or as controller-driven (over an IEEE-488 instrument bus) measurement packages.

The three models—the digital video system, digital multimeter system, and counter/timer system—integrate up to five functions that enhance triggering, improve accuracy, and extend the 2465's applications. The video system incorporates a talker/listener IEEE-488 interface, a counter/timer/trigger, a word recognizer, and an autoranging multimeter. In addition, it can measure television waveforms.



The multimeter system incorporates all the features of the video system, excluding the television capability. The counter/timer system has everything but the TV and the multimeter functions. The packages can be linked to a controller, making the systems suitable for automated testing and waveform analysis.

Applications for the video system include raster-scan-display troubleshooting. The counter/timer can be used in research and development, engineering, and troubleshooting office and business equipment. The multimeter system suits such applications as semiconductor R&D, military applications, and systems integration.

The video system sells for $8,550, the multimeter system for $7,850, and the counter/timer for $6,650. All are available now.

Tektronix Inc., Marketing Communications, P.O. Box 1700, Beaverton, Ore. 97075.
Phone (800) 426-2200 (in Calif., (503) 627-9000) [Circle 357]

Standard-cell line can link with firm's gate arrays

A new family of standard-cell chips and their associated macrocell library, the ISC20000 standard-cell array, uses macrocell functions compatible with the macrocell library of the IGC20000 series gate-array products. This compatibility lets the user move from a gate-array design to a standard-cell design as necessary.

The simplest form of standard-cell chip uses rows of standard-height cells with variable cell widths and variable wiring channels. In addition, the macrocell library includes variable-height macrocells and large macrocells that span multiple rows. Currently, the manufacturer says, the library has over 100 fully characterized Flexicell macrocell functions.

The technology used with the IGC20000 family is silicon-gate CMOS with 2-μm minimum channel lengths and double-level-metal interconnection. A typical delay for a two-input NAND gate is 1.7 ns. Supply voltages may range from 2.0 to 5.5 V, and the family supports the full military temperature range (–55°C to +125°C).

Six different types of packages are available, in addition to a variety of pin counts. Prices will depend on the density of the design and on the packaging and testing required.

General Electric Co., 80 Wolf Rd., Suite 500, Albany, N.Y. 12205. Phone (919) 549-3167 [Circle 370]

Disk pulse detector hunts extremely narrow pulses

Designed for high-density drives that employ such technologies as plated media, thin-film heads, and run-length limited codes, the DP8464 disk pulse detector traces extremely narrow pulses received from the read/write amplifier. The signal amplitude range is from 22 mV peak to peak to 660 mV p-p differential.

The DP8464 converts the analog signals received from the read/write amplifier into digital pulses, indicating to a digital system when changes in the magnetic flux occur. This very large-scale integrated circuit has three main parts: the amplifier, the time channel, and the gate channel. It is designed to reside in the disk drive, with its output directly connected to the DP8460 data separator.

Programmable features include automatic gain-control response, gate-filter channel response, time-channel filter response, comparator hysteresis, and data-output pulse width. The DP8464 is data-rate independent and operates with oxide-coated or plated media, and ferrite or thin-film heads.

Available now, the DP8464 disk pulse detectors are priced at $23.25 each in quantities from 100 to 999.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone (408) 721-5000 [Circle 369]

Two CMOS microcontrollers offer low power consumption

Two 8-bit microcontrollers that operate from power supplies as low as 2.5 V feature three user-optional power-down modes that can reduce power consumption to a few microwatts, the manufacturer says. This low power consumption recommends the IM80C48 and the IM80-C49 chips for those applications that require battery operation, wide voltage operation, or long-term battery backup of on-board random-access memory during ac power interruptions.

The chips are exchangeable with the n-MOS 8048 and n-MOS 8049, respectively; they are said to provide the same speed and performance. They are also interchangeable with other CMOS 8048s and 8049s. Versions with external read-only memory are available.

In 1,000-piece orders, the IM80C48, with 1-K-by-8-bit ROM and 64-by-8-bit RAM, is available 16 weeks after ROM code verification and sells for $6.50 each. The IM80C35, with external ROM and 64-by-8-bit RAM, is available from stock at $4.89 each. The IM80C49, with 2-K-by-8-bit ROM and 128-by-8-bit RAM is available 16 weeks after ROM code verification and sells for $6.50 each. The IM80C39, with external ROM and 128-by-8-bit RAM is available from stock at $4.95 each.

Intersil Inc., 10710 N. Tantau Ave., Cupertino, Calif. 95014. Phone (408) 996-5679 [Circle 371]

Single-chip computer carries 8-bit data converter

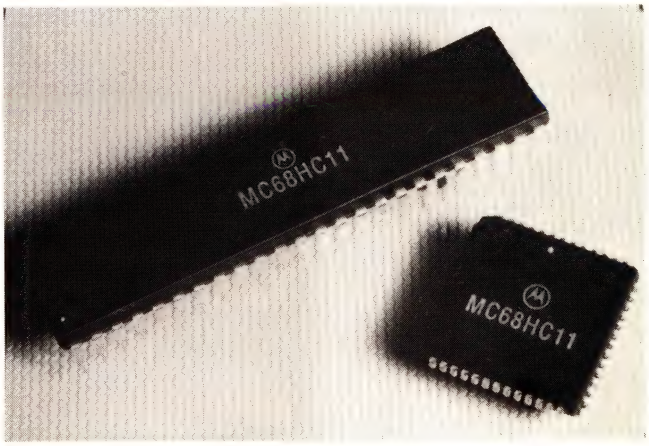
A single-chip microcomputer that offers sophisticated peripheral functions and memory systems on chip utilizes high-performance CMOS technology, which combines the low-power characteristics and high noise immunity of CMOS with the high-speed operation of H-MOS. The MC68HC11A8FN's on-chip memory systems include an 8-K-byte read-only memory, 512 bytes of electrically erasable programmable ROM, and 256 bytes of static random-access memory.

The microcomputer also provides on-chip peripherals that include an 8-channel, 8-bit analog-to-digital converter; a serial communications interface (SCI) subsystem; and a serial peripheral interface subsystem (SPI). The SCI allows the chip to be interfaced with asynchronous peripheral buses such as the RS-232-C. The SPI is primarily intended for simple minimum interconnection input/output expansion; however, it also allows several microcomputers to be interconnected in a multimaster configuration.

A nominal bus rate of 2 MHz runs across a temperature range of –40°C to +125°C. The timer system is expanded to achieve three input capture lines, five output-compare lines, and a real-time interrupt circuit, giving the chip one of the most comprehensive timer systems found on a single-chip microcomputer, the manufacturer says.

The central processing unit is a considerable extension of the MC6801 CPU. In addition to executing all MC6800 and MC6801 instructions, the MC68HCC11A8 uses a four-page op-code map to allow execution of 91 new op codes.

Two basic operating modes, single-chip or expanded-multiplexed, and two special operating modes, bootstrap or special-test, are selectable. The bootstrap puts few or no limitations on the special-purpose program that is boot-loaded into the internal RAM, according to the



manufacturer. This program may be used for such functions as diagnostics on completed modules and for programming the on-chip electrically erasable PROM.

The MC68HC11A8FN is available in a 52-lead plastic leaded chip carrier and soon will be available in a 48-pin dual in-line package. It sells for under $20 in volume quantities. Samples are available now, with production quantities to be available in the second quarter of 1985.

Motorola Inc., Microprocessor Products Div., 3501 Ed Bluestein Blvd., Austin, Texas 78721. Phone (512) 440-2034 [Circle 372]

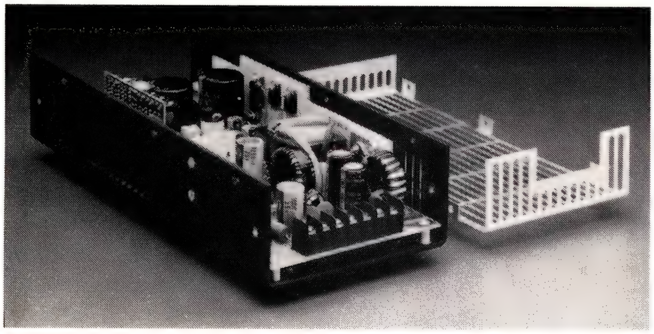
120-W switching supply targets drives and logic

A dual-output switcher, the MASS120-1, offers magnetic amplifier regulation for the secondary output in a 120-W power supply for hard-disk-based systems and peripheral-memory storage systems. The dual outputs are configured for +5 V at 10 A and +12 V at 4 A, with a 6-A peak on the 12-V output, realizing a maximum power of 98 W with 122 W peak.

Additional features include power-fail circuitry and a hold-up time of 50 ms minimum at nominal voltage input and maximum power output. Packaged in an open frame that measures 2.5 by 5 by 11 in., the MASS120-1 also comes with a protective screen.

The unit is available from stock and takes up to eight weeks for delivery through the manufacturer's outlets. In quantities of 1,000, the price is $125 each.

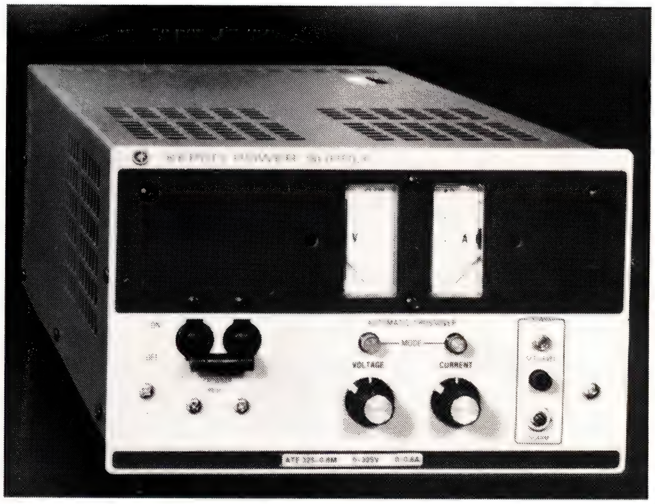
Elpac Electronics Inc., 3131 S. Standard Ave., Santa Ana, Calif. 92705. Phone (714) 979-4440 [Circle 367]



Programmable power supply covers 0 to 325 V, 0 to 0.8 A

Offering wide control over both voltage and current with dc output, the ATE 325-0.8M Power Manager is programmable throughout its range. The unit can be programmed either locally through front-panel rheostats or remotely through a fixed-gain amplifier scaling from an input of 10 V to the rated voltage. Digital input by way of the IEEE-488 bus is possible with the manufacturer's digital interface programmer.

The user may select either slow- or fast-mode operation. In the fast mode, the Power Manager has a bandwidth of 1 kHz and a programming-time constant of 150 µs. The slow mode employs large output and feedback capacitors for the output noise reduction necessary for voltage stabilization; the fast mode bypasses these capacitors, letting the unit follow rapidly changing voltages to deliver a constant current.



The ATE 325-0.8M Power Manager is half-rack size and weighs 43 lb. A single unit sells for $1,706.

Kepco Inc., 131-38 Sanford Ave., Flushing, N.Y. 11352. Phone (718) 461-7000 [Circle 368]

Addition to 4300 family uses two processors

The latest addition to the 4300 family of computers, the IBM 4381 model group 3 has two central processors running under a single operating system. Each processing unit has its own channel and high-speed buffer, but the two share a common main storage.

Thanks to its dual-processor design, the new model group 3 processes commercial appplication workloads at higher throughput rates—1.7 times, according to the company—than the top-of-the-line 4300 processor, the model 4381 group 2. For engineering tasks, the new machine is about twice as fast.

The 4381 uses IBM's recently announced 256-K random-access memory chips to provide from 8 to 32 megabytes of main storage. Also being introduced is a 14-in. color display terminal for the computer, the model 3205.

With 8-megabytes of memory and channels for 12 terminals, the 4381 group 3 will be available in the second quarter of next year at $825,000. An upgrading package for the group 2 sells for $249,420. The monitor, available next month, goes for $2,895.

IBM Corp., Information Systems Group, 900 King St., Rye Brook, N.Y. 10573. Phone (914) 934-4488 [Circle 340]

Add-on turns a terminal into an IBM PC

A 16-bit PC-DOS computer, the Micromix 16 can turn dumb terminals into integrated work stations. The computer can be plugged directly into either IBM Corp. bisynchronous or asynchronous terminals and uses the keyboard and screen to provide access to host computers, or the Micromix 16 can act as a stand-alone computer.

What's more, the computer can run Lotus 1-2-3 concurrently with on-line host operations. When used with IBM 3270-type terminals, the Micromix 16 is attached between the terminals and the terminal controller. When used with non-IBM terminals, connection is made through an RS-232-C interface.

Depending on the type of disk drive and number of ports, the Micromix 16 ranges in price from $2,150 to $3,586. The computer is available now.

Trios Micro Systems Inc., 147 Beacon St., South San Francisco, Calif. 94080. Phone (415) 583-7733 [Circle 341]

Fixturing system requires fewer probes

An automated, computerized fixturing process for bare-board testing, the AFT 1000, automatically assembles and, upon completion of testing, disassembles, a test head utilizing an offset probe. The probe may be reused in different test-head configurations.

The assembled test head is inserted into a vacuum-operated receiver, which may be interfaced with any standard bare-board test system. Complete assembly is typically accomplished within several minutes, regardless of the number of test probes.

The AFT 1000 system is said to require fewer probes and less tester capacity to service a given test area. It also assembles test heads in a repeatable manner and calibrates each test node against a specific tester input/output terminal. In addition, it is said to reduce both dedicated cost and storage requirements of testing to a drilled plate and floppy disk for off-grid boards and to floppy disk alone for standard on-grid boards.

While permitting monitoring of each probe's cyclic lifetime and electronic performance, the AFT 1000 offers stand-alone operation capability in conjunction with small to medium-size testers and integration into computer-integrated manufacturing and computer-aided design and manufacturing systems. Pricing and delivery information were unavailable at press time.

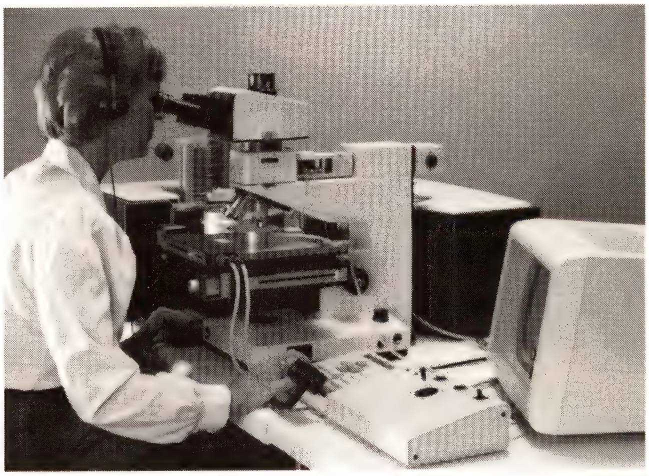
O B Test Group Inc., 487 Jefferson Blvd., Warwick, R.I., 02886. Phone (401) 739-7310 [Circle 350]

Defect-analysis system inspects complex parts

A voice interactive defect-analysis system called Vidas is designed to inspect complex parts such as semiconductor wafers, hybrid integrated circuits, and other assemblies requiring visual inspection.

By controlling the position of the X-Y stage, Vidas moves an object under inspection to a series of positions. At each position, the operator verbally records defects in various categories. As each batch of parts is inspected, a batch report may be printed, listing the total number of defects in each position by category.

In addition to batch reports, the system records defect information on disk for later summary reporting. The summary data is indexed by an inspection-level number so that the system can keep running totals of defect position and categories. Vidas inspection stations may be implemented on a master network station.



An inspection station consists of an IBM Corp. Personal Computer, monochrome display, standard keyboard (for configuration and inspection-pattern creation), a special smaller keyboard (for use during the inspection process), two-axis stepper-motor controller, joystick, printer, and Vidas software.

Technical Instrument Co., P.O. Box 300, 3255 S. Acoma St., Suite 101, Englewood, Colo., 80110. Phone (303) 789-0504 [Circle 351]

Bipolar signal source works as full source or sink

Performing the functions of several instruments, the model 228 is a fully programmable bipolar signal source that can also work as a full 100-W source or sink, in either the constant-current or the constant-voltage mode. An IEEE-488 interface is standard.

The 228 has a battery-maintained nonvolatile internal memory that is capable of storing operating parameters for up to 100 distinct test setups. The memory sequencing can be controlled over the IEEE-488 bus or through the front panel when the instrument is in bench configuration.

In sink operation, the manufacturer says, there is no need to derate power capacity: 100 W is available, with a maximum voltage of 100 V or a maximum current of 10 A. Voltage and current are programmable in three ranges, each with a resolution of 1,000 counts. Output is controlled by an external modulating signal with a dc frequency range of up to 600 Hz.

In the source mode, the modulation signal simulates small ripple or major power fluctuations. In the sink mode, the modulation signal will cause the 228 to act as a variable load that can be used to establish load response of power supplies or batteries.

Test circuits are protected because the 228 powers up in the standby mode, with an output of 0 V and 0 A. When passing from standby to operating mode, the instrument puts out voltage and current according to programmed parameters, thus eliminating large overshoots caused by the source searching for its limits. The load-transient recovery time is less than 1 ms and the output remains stable during and after recovery.

An integral voltage-current monitor gives a 3½-digit reading either on the front panel or over the IEEE-488 bus for use by the controller. The 228 employs a safety disconnect card, which prevents user exposure to live terminals. To gain access to the terminals, the card must be disconnected from the source of power.

With a price of $3,300, the 228 signal source is available eight weeks after receipt of order.

Keithley Instruments Inc., 28775 Aurora Rd., Cleveland, Ohio. 44139. Phone (216) 248-0400 [Circle 362]

Modular unit lets computer acquire and condition data

A modular data-acquisition system called Scadas combines a high-speed, high-accuracy multiplexer with an analog-to-digital converter and signal-conditioning modules, such as programmable precision filters and amplifiers. Mainframes are available with from 8 to 32 dual-channel modules and 16- to 64-channel multiplexers; synchronization outputs are available to increase the system to over 64 channels. Scadas incorporates both the IEEE-488 and the RS-232-C interfaces, and can connect with any minicomputer or microcomputer.

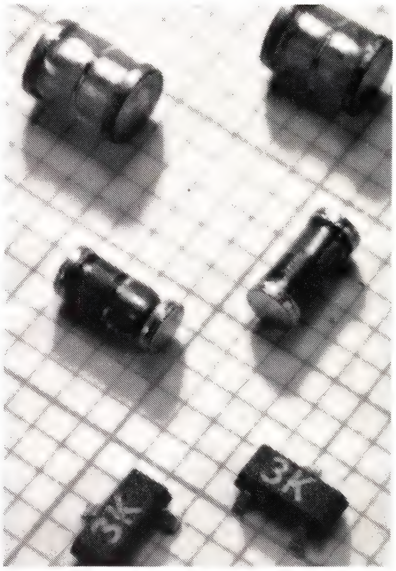
The throughput rate for 16 channels is 300 kHz (3.3 μs conversion time). Parallel sampling avoids time-skew effects, and the minimum sample rate is 3 μs times the number of channels plus 6 μs. The 10-MHz crystal-controlled clock is programmable. Triggering is either internal or external and is completely programmable. With internal trigger, the level is selectable in 14 steps.

A first-in, first-out buffer avoids timing problems. A 16-channel unit with filters is priced at from $12,000 to $15,000.

Structural/Kinematics, 950 Maplelawn, Troy, Mich. 48084. Phone (303) 643-4622 [Circle 366]

Component family comes in surface-mountable packages

A range of surface-mounted devices is offered in metal-electrode face-bonding (MELF) or cylindrical mini-MELF and TO-236 chip form. Products include transistors, 1-A standard and fast rectifiers, and silicon oxide capacitors, as well as universal, tuner, switching, band-switching, Schottky, 500-mW, and 1-W zener diodes. The SMD family is supplied prepackaged on industry-standard 8-mm or 12-mm tape, suitable for use with high-speed automatic-placement equipment. Alternatively, components can be supplied loose, at a lower cost.



To meet electronic, mechanical, and environmental specifications, all of the diodes are hermetically sealed in glass packages and are individually tested. Technical support, consisting of specific advice on production quality assurance as well as the use of automatic-placement equipment, is offered.

Prices depend on the type of device, and will be quoted by the manufacturer. The line of components is available now for immediate delivery.

ITT Semiconductors, 500 Broadway, Lawrence, Mass. 01841. Phone (617) 688-1881 [Circle 365]

Dot-matrix printer handles bit-mapped graphics

Compatible with all computers from its manufacturer and more than a dozen microcomputers from other companies, the Letterprinter 210 delivers high-resolution bit-mapped graphics following protocols used by both Digital Equipment Corp. and IBM Corp. Draft-quality text is handled at the rate of 240 characters/s and near-letter-quality text at 40 characters/s.

An optional, user-installable IBM/Centronics parallel interface connects the Letterprinter 210 to many popular personal computers. The Letterprinter 210 can selectively emulate the IBM Graphics Printer and the Epson MX80 with Graftrax printer. Plug-in cartridges are required for each emulation mode, and emulation configuration switches are located on the printer.

The print head's laminated-core technology pulls less current, resulting in cooler operation, extended print-head life, and improved print quality, the manufacturer says. Lifetime expectancy for the print head is claimed to be more than 500 million characters.

The noise level of this printer is 58 dB, compared with an average level of 68 dB for dot-matrix printers, the manufacturer says. It accepts up to four-part forms, and an optional bidirectional forms tractor allows the user to add subscripts, overlay graphics, or produce other special printing jobs.

The Letterprinter 210 is supported by the manufacturer's library of more than 30 typefaces and character sets, in addition to having a wide range of software.

Volume quantities of the Letterprinter 210 are being shipped now. The list price is $1,595. A package of two font cartridges and the parallel interface is available for $125; other font cartridges are priced separately. The sheet feeder is priced at $595, the bidirectional forms tractor at $295.

Digital Equipment Corp., Terminals Business Unit, 129 Parker St.,
Maynard, Mass. 01754. Phone (800) 344-4825 [Circle 378]

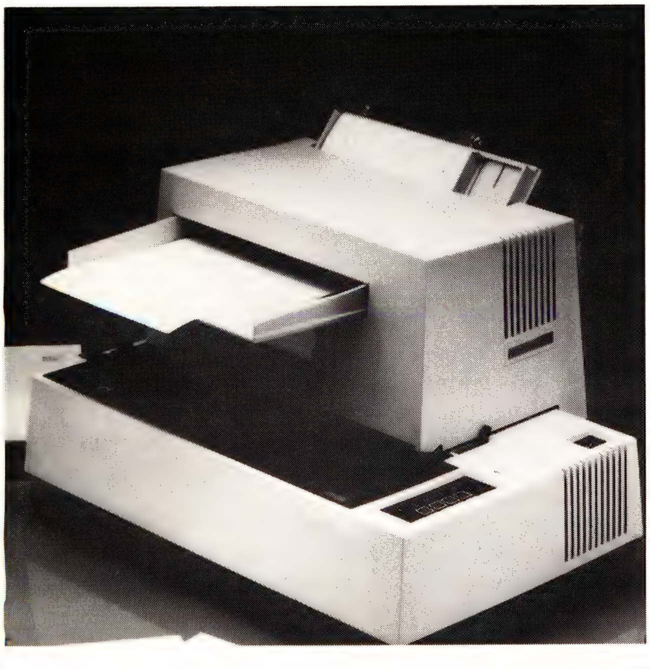
Printer plus sheet feeders gives price break to offices

With prices starting at $1,895 for a 90-copies/s daisy-wheel printing and paper-handling system, the manufacturer claims a price-to-performance breakthrough for the Primage 90 and its accompanying Pagemate sheet feeder. A method called "print in flight" allows continuous work flow rather than stopping and starting the print head for each letter.

The result is said to be not only increased speed over other available printers but also reduced wear, less noise, and improved registration. The unit prints bidirectionally, with proportional spacing, and at 10-, 12-, and 15-pitch settings. The printer offers horizontal spacing in increments of 1/120 in. and vertical spacing at 1/96 in. Printing can be done on continuous computer forms or on individual sheets.

The Pagemate sheet feeder is available in a two- or three-bin model. It boasts a short paper path, and it forward-collates paper and envelopes. Sheet feeders get their commands from the computer, or commands can be added to the text by the operator.

Three systems are offered: the Primage 90 printer with Pagemate I single-sheet feeder, $1,895; the Primage 90 with Pagemate II two-sheet feeder, $2,095; and the Primage 90 with Pagemate III two-sheet feeder plus envelope feeder, $2,295. The two-bin feeder can be changed to a three-bin feeder for an extra $250. Delivery on all items will be made in the first quarter of 1985.



Primages Inc., 620 Johnson Ave., Bohemia, N.Y. 11716.
Phone (516) 567-8200 [Circle 377]

Oscillographic recorder is controlled through IEEE-488

A microprocessor-based, modular oscillographic recorder, the model 3410, has all its functions under the control of a test system using an IEEE-488 interface. Preamplifiers include dc voltage, temperature, dc bridge, frequency voltage, and fixed root-mean-square amplitude.

Employing a thermal-pen recorder, the 3410 features rectilinear recording systems, frequency response to 145 Hz (–3 dB), and a choice of 50- or 100-mm writing-width galvanometers.

Other options include an interval-trigger module that adjusts the trigger threshold of the recorder; once triggered, the recorder will operate for the preprogrammed length of time. In this way, the 3410 may be left to record a transient signal over a period extending from days to weeks.

Depending on user configuration and options, the price of the 3410 oscillographic recorder starts at $5,725. The recorder is available now.

Soltec Corp., 11684 Pendleton St., Sun Valley, Calif. 91352.
Phone (800) 423-2344 (in California, [818] 767-0044) [Circle 376]

Mobile system calibrates multimeters, test gear

A mobile automatic calibration system, the 4100 Portocal, is designed for *in-situ* calibration of multimeters and automatic test equipment. It is said to push standard laboratory accuracies into the production environment.

Connection to the unit is simplified by the isolation available at the front of the terminal of each calibrator. This allows two sets of calibrator terminals to be bused together to form a single analog highway, removing the need for external switching.

The Portocal system comes with software, compatible with IBM Corp. Personal Computers, that is designed for multimeter calibration. Menu screen formats prompt the user through predefined calibration procedures, said to provide greater repeatability and improved documentation. Pricing and delivery information was unavailable at press time.

Cooper-Cameron Inc., 9 Village Sq. E., Clifton, N.J. 07011.
Phone (201) 546-2262 [Circle 375]

Turnkey test systems calibrate meters on site

A mobile calibration system designed for on-site accuracy checks of voltmeters, ammeters, ohmmeters, and multimeters, the Calcart can be wheeled to a work location and used without interrupting production. Its operation is controlled by an IBM Corp. Personal Computer with color display and 256-K bytes of random-access memory, and it can be configured with a variety of stimulus units.

Stimuli range from 1 µV to 1,200 V dc, and from 1 mV to 1,100 V ac over a frequency range from 10 Hz to 1 MHz; also ac and dc currents ranging from 20 µA to 100 A at frequencies to 10 kHz.

Calibration can be performed on meters that are IEEE-488 bus talkers and listeners or talkers only; non-IEEE and non-binary-coded-decimal (BCD) units; BCD talkers and listeners; and BCD talkers only.

Calcart model 4050A-mod 101 includes a Fluke 5200A ac voltage calibrator and a Valhalla 2701B dc voltage calibrator, as well as the manufacturer's 1620A transconductance amplifier. Its price is approximately $29,950, but this varies according to the customer's choice of configuration. Delivery takes up to four to six weeks after ordering.

Calcart model 4003A-mod 101, a mobile automated oscilloscope-calibration system, incorporates the manufacturer's 6127B programmable oscilloscope calibrator, with a bandwidth range to 1 GHz. It is also priced at $29,950. Delivery is in three to five weeks.

Ballantine Laboratories Inc., P.O. Box 97, Boonton, N.J. 07005.
Phone (201) 335-0900 [Circle 374]

8-bit video converter available at low cost

Selling for $18.11 in 100-piece quantities (3-count accuracy), the TML1842B digital-to-analog video converter is offered as a bargain for graphics terminals. It is packaged in a 20-pin plastic dual in-line package that is 0.3 in. wide for minimal board space.

The TML1842 has composite synchronization, composite blank, and 10% bright signals. Driving the red, green, and blue video guns, it handles 75-Ω or 37.5-Ω loads while operating at a minimum conversion rate of 25 ms/sample. The converter has 1-bit linearity, requires a single +5-V power supply, and is compatible with TTL and CMOS.

The TML1842A, in a 20-pin plastic package and with a 2-count accuracy, sells for $20.12 each in 100-piece lots. Delivery of both converters takes two weeks.

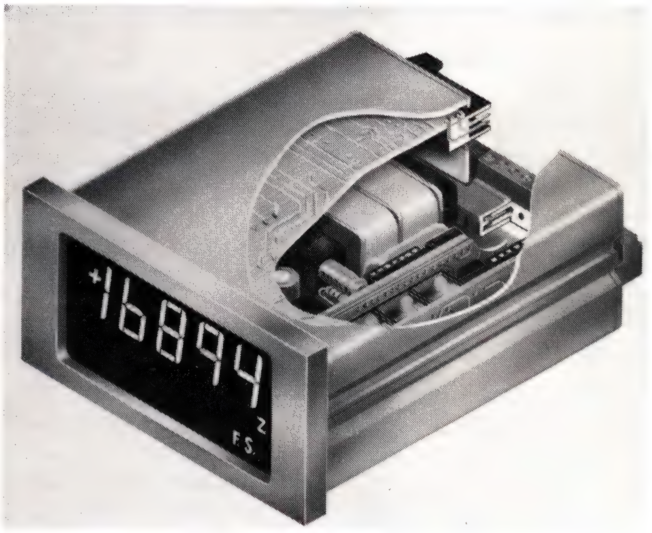
Telmos Inc., 740 Kifer Rd., Sunnyvale, Calif. 94086.
Phone (408) 732-4882 [Circle 373]

Individual cards customize digital panel meter

The Universal model digital panel meter is configured with a mainframe plus five display types, excitation and analog output options, input signal conditioning, and more, for flexibility in user-selected applications.

The Universal's mainframe possesses ±0.005% accuracy, and linearity to ±4½ digits (analog to digital). The RS-232-C, RS-422, and IEEE-488 interfaces are available on the Universal. Excitation and analog output options accommodate most industry-standard transducers, the manufacturer says.

A temperature signal conditioner is available for both platinum and copper elements, as well as for thermistors and monolithic integrated-circuit temperature detectors.



The standard housing for the Universal is metal-filled plastic with 4 Ω/in.^{2} conductivity and electromagnetic and radio-frequency interference attenuation of 70 dB at 0.5 MHz. Other housing options are available.

In quantities of one to nine, the Universal is priced at $200; discounts are offered for larger orders. Shipment will be made from stock.

International Microtronics Corp., 4016 E. Tennessee St., Tucson, Ariz. 85714. Phone (800) 847-8478 or (602) 748-7900 [Circle 380]

Small, ruggedized meter runs on a 5-V power source

Taking up less than 3.9 in.^{3} back-of-panel space and less than 1.8 in.^{2} when mounted on the front, the D display digital panel meter has a low power requirement of 5 V. The ruggedized display is encapsulated for protection against moisture, corrosive fumes, vibration, shock, and acceleration. The standard model weighs about 3 oz., the ruggedized model about 5 oz. They operate in temperature ranges of –10°C to +70°C and –40°C to +85°C, respectively. The height of the character display is 0.3 in.

Velonex, 560 Robert Ave., Santa Clara, Calif. 95050.
Phone (408) 727-7370 [Circle 379]

Single board integrates the CPU with peripheral control

Single-board computers, a fallout of large-scale chip integration and tighter board layouts, are becoming much more than just number crunchers with their own memory. Many complex printed-circuit-board computers are beginning to bear more peripheral-control functions than central-processing-unit circuitry.

With the introduction this week of a 68010 microprocessor-based 11-by-14-in. module, the CPU-peripheral integration trend has turned Interphase Corp. into a computer supplier. Until now, the firm specialized in controllers for storage peripherals.

NEC's on-screen character displays reach out and grab attention.

ome video products look pretty
uch alike to customers
stores. On-screen character
isplays are a sure way to make
our products stand out and in-
rease sales appeal.
NEC offers two types of ad-
anced CMOS LSIs that can be
ilored to your new ideas. They
nable you to create attractive,
n-screen time, channel number,
mer status and other informa-
on displays. Also, convenient
ate, title and recording data
isplays for VCRs and cameras.

The μPD6104C displays 12 characters (6×2 lines) from a 16-character vocabulary, while the high-end μPD6105C puts 70 characters (14×5 lines) on-screen using a 58-character vocabulary. Any letters, numerals, signs or symbols can be included. Smart 5×7-dot characters, with smoothing quarter dots, assure fine clarity. In seven colors, even with a black background or fringe. Height and location are selectable.

Make your TVs, VCRs and cameras stand out—install NEC's on-screen character displays.

NEC Electronics Inc.
401 Ellis Street, Mountain View, CA 94043.
Tel: 415-960-6000. TWX: 910-379-6985.

NEC Electronics (Germany) GmbH
Tel:0211-650302. Telex:8587419 NEC D.

NEC Electronics (UK) Limited
Tel:0698-732-221. Telex:777565 NEC UKG.

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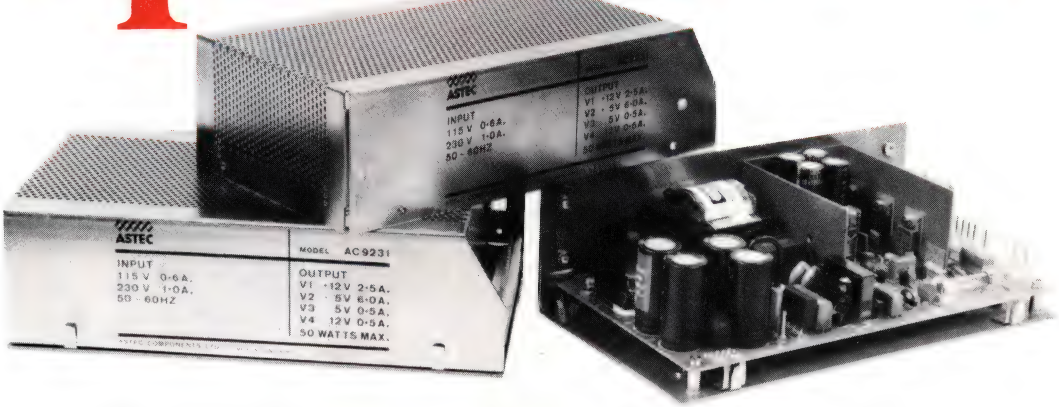
NEC Corporation
Tokyo, Japan

The World's Third Super Power



With over 5 million power supplies in use throughout the world and current production levels exceeding 300,000 per month, we are undoubtedly a leader in the field of switching power supplies. We have several hundred types in our range covering power limits from a few watts to hundreds of watts, many with an MTBF approaching 100,000 hours.
Our PCB's form the basis for many personal and small business computers and we have delivered more than 10 million modulators for use in microcomputer and television games.
Add this to our die attach and lead bonding facilities, plus more exciting new products to be announced this year, and you'll see who is the real power!

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See us on Stand No. 16, Hall 7,
at ELECTRONICA (Nov. 13th - 17th)

Circle 108 on reader service card

Cool Chips

So cool,
so fast,
and SO small.

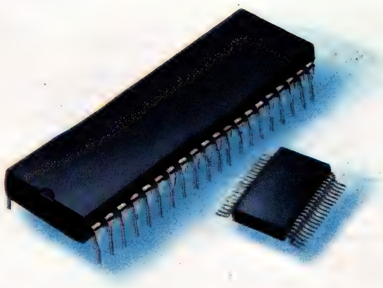
And so many! Nearly 300 high-speed CMOS logic chips. More than any other vendor. We ship more, too – and in space-saving SO mini packages as well as DIL!

Use the HCT types as drop-in replacements for LSTTL – you'll find they dissipate much less power – even at their highest operating speed.

Use the HC types for new designs and add the advantages of their wide voltage range and high noise immunity to the high speed. We guarantee 30 MHz, but it's typically 60.

What's more, we've proven processes, too! We've been running polysilicon for more than ten years. Now, with tighter design rules, we're delivering 3 μm gates that clock-up five times the speed at a tenth of the power of early CMOS – and they're latch-up proof to 100 mA.

For data and samples contact:
Philips Electronic Components
and Materials Division,
5600 MD Eindhoven,
The Netherlands.



Philips put the PC74 HCMOS families in standard DIL packages as well as in the space-saving SO mini packs. The comparison shown here is between 40-pin DIL and 40-pin SO.

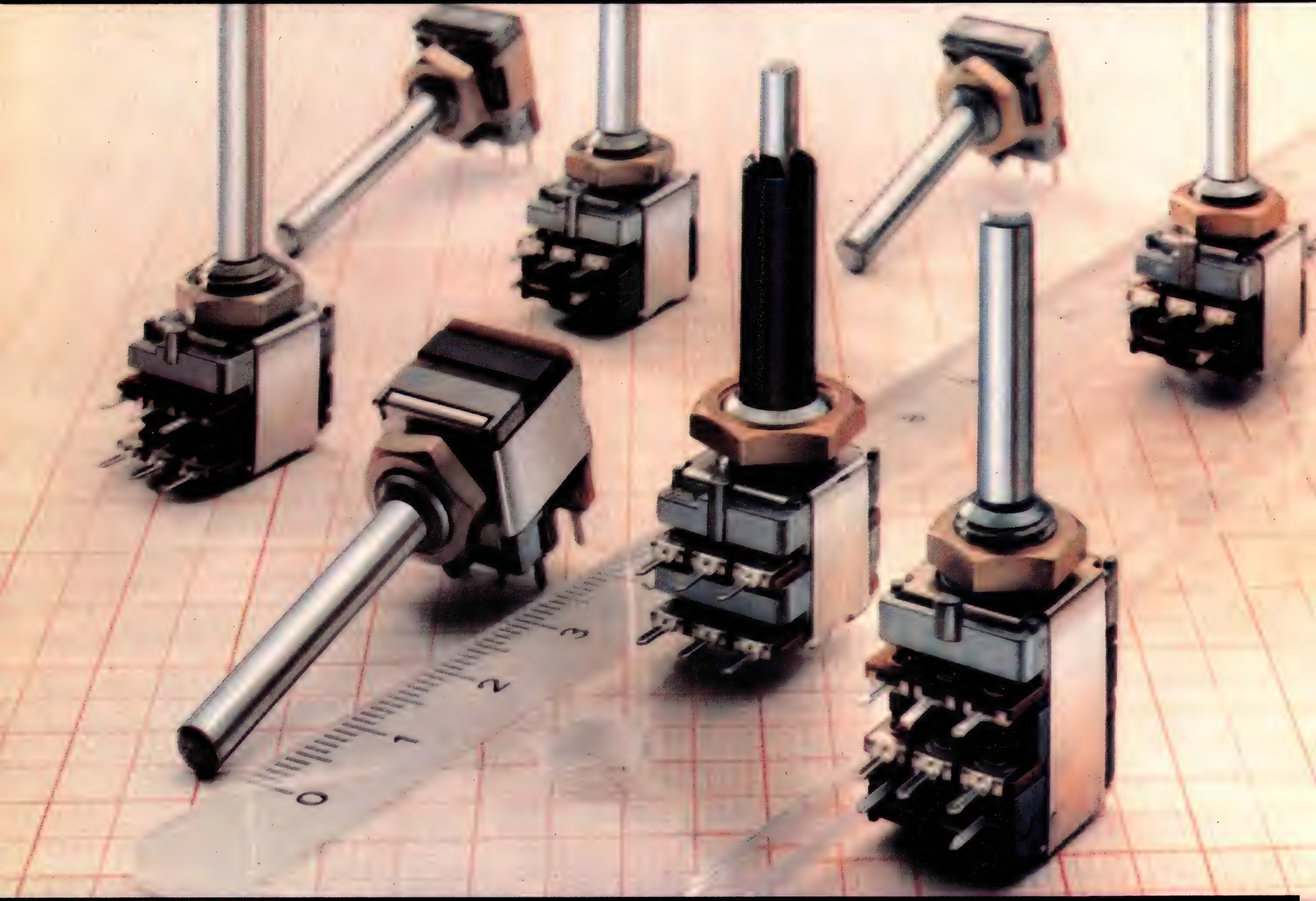
Making the Most of CMOS

PHILIPS

PHILIPS
Electronic
components
and materials

Circle 109 on reader service card

Preh



PREOSTAT 12 Drehpotentiometer

Die wirtschaftliche Antwort an qualitätsbewußte OEM's
kleiner – kompakter – zuverlässiger

Baubreite 12 mm
Wahlweise 1 oder 2 Wellen
Belastbarkeit 0,05 W (lin), 0,025 W (log)
Nennwiderstand 100 Ohm – 4,7 MOhm (lin + log) E3
Temperaturbereich – 40°C bis + 80°C

Neue Technologien:

Schlupf- und ruckfreies Einstellen
Zuverlässig durch alterungsbeständige Anschlußtechnik
Automatisierte Fertigung – kontinuierliche Qualität!

Potentiomètre rotatif – Preostat 12

La réponse économique pour l'OEM conscient de la qualité
- plus petit – plus compact – plus fiable –

- Largeur 12 mm
- En option avec une ou deux axes
- Charge admissible 0,05 W (lin) – 0,025 W (log)
- Résistance nominale 100 Ohm – 4,7 MOhms (lin + log) E3
- Plage de température – 40°C à + 80°C
- **Technologie nouvelle:** fonctionne sans glissement et sans à-coups

  fiable en raison de sa technique de connexion non-vieillissante

  fabrication automatisée, donc qualité uniforme du produit

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OEM's
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- Nominal resistance 100 Ohms – 4.7 MOhms (lin + log) E3
- Temperature range – 40°C to + 80°C
- **New technologies**
  - smooth shaft rotation, n slipping or jerking
  - reliable connection between the resistive element and solder terminals, not affected by aging
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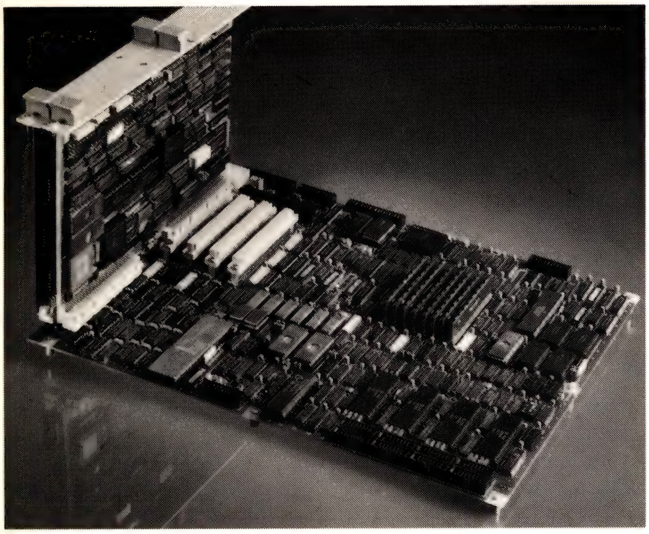
Circle 110 on reader service card



With a high level of integration, the baseboard computer touts not only a 10-MHz 68010 but also up to 2 megabytes of dynamic random-access memory, memory management, programmable timers, a 68008-based disk controller for both floppy-disk and Winchester drives, serial and 8-bit ports, support for AT&T Bell Laboratories' Unix operating system, and five VMEbus expansion slots. The board can serve up to eight users with its serial ports, each of which handles 19.2 kb/s concurrently or a total of 1 Mb/s simultaneously. The module also accommodates 18 megabytes of virtual memory.

In all, the multiuser/multitasking single-board computer foundation system represents the circuitry usually found on nine different boards, says the company. The baseboard computer sells for $5,995, as opposed to the $12,000 a comparable multiboard computer system would cost, according to the firm. Part of the trick to fitting so much on the board is the use of several semicustom chips resident on Interphase's controllers. Volume deliveries are slated to begin in January 1985.

Interphase Corp., Merrell Rd., Dallas, Texas 75229.
Phone (214) 350-9000 [Circle 382]

With battery-backed RAMs, board retains data 10 years

With static random-access memory chips, teamed with lithium battery cells inside dual in-line packages, an STD-bus board from Mostek Corp. retains up to 16-K bytes of data for at least 10 years without any power. The firm says this makes the STD-bus memory board an extremely cost-effective nonvolatile storage module.

The MDX-ZRAM board contains the company's 2-K-by-8-bit MK48Z02 Zeropower RAMs [*Electronics,* May, 5, 1983, p. 47]. The boards come with 4-, 8-, and 16-K bytes of battery-backed storage. The board can also accommodate future 8-K-by-8-bit Zeropower RAMs, when available, bringing the total amount of possible nonvolatile storage to 64-K bytes.

"Calculations indicate that nominal retention would be around 30 years," notes Jerry Roop, STD-bus product line manager in Carrollton, Texas. Unlike other STD cards featuring battery-backed RAMs, Mostek's newest memory module offers more nonvolatile storage because board space is not taken up by discrete batteries. The batteries-in-a-DIP chips also integrate the power-down circuitry on the CMOS die, explains Roop.

The ZRAM board has access times of 150 ns and supports 4-MHz bus operations without wait states. The memory module carries the same operational temperature range as standard Mostek STD cards—0°C to 60°C. The boards are targeted at a number of applications, including industrial automation where the battery-backed memories would retain processing-state data should a power failure occur. Roop also suggests that ZRAM boards could be loaded with programs, unplugged, and placed into factory-floor systems without loss of software.

In quantities of less than 10, the 4-K-byte MDX-ZRAM boards sell for $250 each. With 8-K bytes of Zeropower RAM, the ZRAM boards sell for $295 each. The 16-K-byte board sells for $375. Boards are now available for volume deliveries.

Mostek Corp., 1215 W. Crosby Rd., Carrollton, Texas 75006.
Phone (214) 466-6027 [Circle 381]

Board adds ports, memory to IBM PC AT systems

With a multifunction memory-expansion board for the IBM Corp. Personal Computer AT, users can add up to 3 megabytes of random-access memory to take full advantage of the IBM PC AT's high-performance bus and larger memory-addressing capability. The user-upgradable memory holds either standard 64-K or 256-K chips.

In addition, the board, called Advantage!, offers up to one parallel printer port, two serial ports, and a game port. The board, with 128-K bytes of memory, will sell for $495. Volume quantities are available now for immediate delivery.

AST Research Inc., 2121 Alton Ave., Irvine, Calif. 92714.
Phone (714) 863-1333 [Circle 383]

48-channel logic analyzer suits bit-slice processors

A logic analyzer that offers 48 channels at 100 MHz is useful for high-speed bit-slice microprocessors, emitter-coupled-logic circuits, gate arrays, and discrete logic designs. The model K205 features 16 independent triggering-decision levels, each of which has four commands. Four decisions can be made every 20 ns, enabling designers to locate difficult logic problems by triggering a unique event.

Trigger points can be chosen while running at full speed through logic sequences, without restrictions. Called Trace Control, the method is 150% faster than comparable selection schemes, the firm says. The K205's tolerance-compare feature allows fast analysis of logic circuits by comparing timing sequences against stored references, thereby eliminating sampling-error differences found in asynchronous analysis.

A glitch-mode feature displays noise on all channels for faster identification of problems, and a latching scheme maintains full channel width and memory depth when using the glitch mode. Three separate measurement-input sections monitor independent circuit clocks for multiprocessor systems.

Priced at $14,000 for a single unit, the K205 can be delivered in six weeks.

Gould Inc., Design and Test Systems Division, 4600 Old Ironsides Dr., Santa Clara, Calif. 95050.
Phone (408) 988-6800 [Circle 359]

State/timing analyzer aids in bit-slice designs

Performing state analysis at rates of up to 125 MHz and timing analysis for up to 32 input channels, a unit makes measurements for bit-slice, state-machine, and high-speed-microprocessor designs. With the analyzer, the firm's 64000 logic-development system supports analysis for products using very high-speed logic.

Features of the HP 64610S focus on measurements for high-speed custom and proprietary hardware applications with very fast logic circuits, and also include timing analysis extending to 400 MHz in a fast-sample mode, 200 MHz for wide sample, and dual-threshold and glitch modes. It also offers 8, 16, 24, or 32 input channels for either synchronous or asynchronous analysis, and three modes, each with a 4-K deep memory, and a fast-sample mode with an 8-K deep memory. Existing HP 64600S analyzers can be upgraded with the new features.

Prices for the HP 64610S range from $7,000 to $20,000. Deliveries take 12 weeks.

Hewlett-Packard Co., Inquiries Manager, 1820 Embarcadero Rd., Palo Alto, Calif. 94303 [Circle 360]

Spectrum analyzer covers video band to ultraviolet

A spectrum analyzer, the model MS 610A, covers frequencies from the video band to the ultraviolet—10 kHz to 2 GHz. The compact, lightweight analyzer offers an IEEE-488 interface for remote operation, coupling function for greater measurement efficiency, and a digital display with a peak-value center function.

Applications include spectrum analysis for product design, oscillation, and distortion measurements of active elements and circuits, spurious-signal measurements for production control, panoramic reception of radio waves, and measurement of noise radio waves.

When connected to the firm's tracking generator and a bridge, the analyzer can measure impedances and transmission characteristics of amplifiers and other devices. The analyzer's specifications include a dynamic range of –115 dB or less, a resolution bandwidth of 1 kHz to 1 MHz, and a sweep time of 10 ms to 10 s stepped.

Scheduled to be available in April 1985, the MS 610A sells for $6,355.

Anritsu America, 128 Bauer Dr., Oakland, N.J. 07436.
Phone (201) 337-1111 [Circle 361]

Transfer system moves 20-by-18-in. boards quickly

A printed-circuit-board transfer system, the Dynapert Board Loader/Unloader automatically moves bare pc boards from a storage magazine to an insertion or surface-mounting machine and then returns assembled boards to their original slots. The entire operation is performed in just 5 s, the company claims.

Compatible with many automatic assembly machines and materials-handling systems and magazines, the system holds up to 60 boards or pallets measuring 20 by 18 in. The system digitally displays the number of each magazine slot being loaded and can accept magazines from a wide range of materials-handling systems.

The transfer system is priced starting at $28,000, depending on configuration.

Dynapert, 181 Elliot St., Beverly, Mass. 01915.
Phone (617) 927-4200 [Circle 344]

System prints labels to be heat shrunk on wires

A wire-identification system eliminates the fuss associated with marker-and-masking-tape hand-labeling methods. Called the Bradywriter, the microprocessor-controlled dot-matrix printer has enough memory to store and print 75 legends at a time. The labels can then be applied and shrunk on the wire by using the company's Bradysleeve applicator.

Users can create their own labels on the spot and they can also stock the Bradysleeve markers they use most frequently. The Bradywriter printer is easier to learn than a computer, the company says: generating labels is done with just a few commands.

The 22-lb unit's color-coded keyboard is sealed to protect it from the dirt and moisture typically found in industrial environments. The system prints up to 100 characters/s, printing eight characters/in. vertically and a choice of 10 or 20 characters/in. horizontally. The Bradywriter printer also prints legends in capital letters, numbers, and symbols in either standard or boldface type.

W.H. Brady Co., Industrial Products Division, 2221 W. Camden Rd., P.O. Box 2131, Milwaukee, Wis. 53201.
Phone (414) 351-6630 [Circle 345]

System provides illumination for wire and die bonders

Using a principle of electro-optic light control, the MDC-2000 illumination system provides standard illumination at the long working distances required for wire and die bonders (25 to 50 mm, or 1 to 2 in.) while permitting the rapid determination of wire-bond integrity for quality-control purposes.

The illumination system may be adapted to most wire and die bonders and standard inspection microscopes. System costs range from $2,000 to $4,000.

Microscopy Development Corp., 6300 Telegraph Ave., Oakland, Calif. 94609. Phone (415) 654-2410 [Circle 346]

Software plus DAC gives any microprocessor speech

Designers can get high-quality speech synthesis on any 8- or 16-bit microprocessor by using patented algorithms. All that must be added to the microprocessor is an 8-bit digital-to-analog converter along with the appropriate filtering and audio amplification.

The company claims that replacing a speech synthesizer with an 8-bit DAC not only reduces the cost of the speech-synthesis subsystem, it provides a more flexible approach than an integrated-circuit-based speech synthesizer. Unlike hardware, the software-based synthesis can be tailored to suit a particular application.

The algorithms can be optimized over a wide range of speech-quality and data-rate options, and even special outputs such as the A-law and μ-law standards used in digital telephony can be incorporated. In addition, software-based speech can improve as fast as the speech research, since there is not the lag inherent in IC designs, the company claims.

The algorithms produce high-quality speech in the data-rate range of 2 kb/s to 5 kb/s. Speech anywhere in this range is intelligible, natural, and carries the personality of the original voice.

The charge for algorithm development depends on the target microprocessor and the degree of customization required for the specific application. Royalties range from $10 per unit for manufacturing quantities under 100 to $1 per unit for manufacturing from 50,000 to 100,000.

Electronic Speech Systems, 2991 Shattuck Ave., Suite 301, Berkeley, Calif. 94705. Phone (415) 644-8126 [Circle 342]

Board gives speech capabilities to IBM PC

An integrated plug-in board for the IBM Corp. Personal Computer, the Sar-10 Voice-Plus provides both voice recognition and audio response. The voice-recognition function uses a custom very large-scale integrated-circuit chip set with 250-word capability.

Spoken inputs are digitized, and user-defined ASCII outputs are sent to the PC, thereby providing what is, in effect, a voice keyboard. A high-quality speech chip digitally reproduces speech as well as other sounds. A 256-K random-access memory stores more than 65 s of audio response at 32 kb/s.

Utility programs provided with the board allow input and output capabilities to be integrated easily into new and existing software applications. The Sar-10 is priced at $1,490 each; discounts for volume purchases are available.

NEC America Inc., 8 Old Sod Farm Rd., Melville, N.Y. 11747.
Phone (516) 753-7000 [Circle 343]

MATERIALS ☐ SUPPLIES ☐ ACCESSORIES

Stainless-steel-loaded fiber compounds that prevent static-electricity buildup also offer shielding from electromagnetic interference. The manufacturer says that use of this product allows conductivity and EMI shielding to be molded into a plastic part rather than being added as a secondary metal coating. The material is specified with a loading of 5 weight/percent, which achieves conductivity without significantly affecting the base resin's tensile, flexural, or impact strength or its elongation properties.

Wilson-Fiberfil International, 2267 W. Mill Rd., P.O. Box 3333, Evansville, Ind. 47732. Phone (812) 424-3831 [Circle reader service number 421]

A video-display filter in leaded acrylic, the I-Protect, will block up to 97.7% of radiation emissions, the manufacturer says. It will also block up to 80% of static charge. A scratch-resistant coating covers the leaded acrylic, and a circular polarizer enhances contrast. The filter is mounted with Velcro strips.

I-Protect Inc., P.O. Box 90235, World Way Center, Los Angeles, Calif. 90009. Phone (213) 215-1664 [Circle 422]

Two cables are offered to electronics systems installers: the model 9868 synchronous interface cable, conforming to RS-232-C requirements for interconnection to synchronous modems, and a high-flex version of 0.050-in. pitch-laminated flat cable, for use in high-speed printers and robotics applications.

The 9869 has fourteen 28-AWG stranded tinned-copper conductors, each individually wrapped with an aluminum-polyester foil shield and a 28-AWG copper drain wire. The representative price is $580.80 for a 1,000-ft putup.

The high-flex flat cable is available with 10 to 64 28-AWG (19 by 40) silver-plated, stranded copper alloy conductors on 0.050-in. spacing. The temperature range is —20°C to +105°C, and the voltage rating is 300 V rms. In quantities of 1,000 ft, a 26-conductor cable would be priced at $302.48 per 100 ft. Both cables are available from stock.

Belden Electronic Wire and Cable, 2000 S. Batavia Ave., Geneva, Ill. 60134. Phone (312) 232-8900 [Circle 425]

Flux is removed from printed-circuit boards and assemblies by Micro Care aerosol solvent, in a method that the manufacturer says combines soaking, scrubbing, and flushing in the same operation. The base for most items in this line is Genesolv D, said by the manufacturer to have low toxicity and to be nonflammable and nonconductive when blended with stronger solvents and alcohols. The Spray-Thru-Brush technique releases only as much solvent as is required for the job at hand, with no standby evaporation.

Genesolv Solvent Systems Group, Allied Corp., P.O. Box 1139R, Morristown, N.J. 07960. Phone (201) 455-6751 [Circle 433]

Tools for contact connector insertion, removal, and crimping for military or commercial applications, are available both as standard items or designed to user specifications. The manufacturer requests that drawings, samples, or specifications for tool kits be forwarded with inquiries.

Jonard Industries Corp., Custom Products Div., 134 Marbledale Rd., Tuckahoe, N.Y. 10707. Phone (914) 793-0700 [Circle 432]

A urethane-based conformal coating, Nordbak 9821, is designed to protect printed-circuit boards and components from moisture, dust, corrosion, and vibration, and is said by the manufacturer to offer excellent cured electrical properties. A 1-mil film build is obtained by either spraying or dip coating in one application.

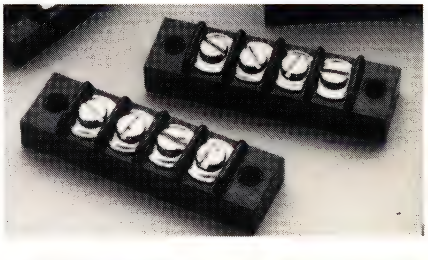
Rexnord Chemical Products Inc., 6120 E. 58th Ave., Commerce City, Colo. 80022. Phone (303) 289-5651 [Circle 426]

An antistatic kit that includes a workbench mat, grounding cable, and wrist strap and coil cord is offered for the protection of solid-state components. The wrist strap is detachable from the coil cord, permitting each operator to use his or her own wrist strap at the work station. The kit, stock No. 162351, is available from RCA parts distributors.

RCA, Distributor and Special Products Division, 2000 Clements Bridge Rd., Deptford, N.J. 08096. [Circle 424]

Two series of single-row barrier terminal strips, rated at 10 and 30 A respectively, may be inspected under the manufacturer's free-sample offer. The 23000 series has its terminals spaced on ¼-in. centers. Barrier height is 0.31 in. and width is 0.41 in. They can be furnished with up to 22 circuits. The 26000 series, with terminals spaced on 9/16-in. centers, 0.72 in. high and 0.75 in. wide, can be furnished with 18 circuits.

Vernitron Corp., Beau Products Division, P.O. Box 10, Laconia, N.H. 03247. Phone (603) 524-5101 [Circle 427]



Letters

Byte-size wafer

To the editor: Sinclair's intent to field a wafer disk memory [*ElectronicsWeek,* Sept. 10, 1984, p. 18] would seem to resurrect a controversy resolved over a decade ago between serial and random-access semiconductor chips. A wafer of byte-wide bus-interconnected RAMs (with bad RAMs treated as unavailable virtual-memory pages) has the same advantages as a serial wafer—low cost, fail-safe reliability, low power, and compactness—but with the speed of a random-access main memory.

Gilman D. Chesley
Los Altos, Calif.

Aiming for accuracy

To the editor: In the article reporting on developing a voice-activated typewriter ("AI pioneer talks up voice-activated typewriter," *ElectronicsWeek,* Oct. 22, 1984, p. 83), you report, "For example, if [Raymond Kurzweil's speech-recognition machine] hears a verb, it might expect a preposition to follow. If the preposition happens to be 'for,' the voice-activated typewriter will know to print 'for' rather than 'four.' "

Good luck to Kurzweil, although he faces enormous problems. Look at these examples using the same verb: The quartermaster aimed for low inventory. The execution squad aimed four rifles.

We ran into these problems while designing a tutorial program that accepts freeform responses to questions and grades them. We will soon complete an application that we targeted by focusing our goal, which Kurzweil will likely do, too.

Charles Pine
Wordcraft
Oakland, Calif

Correction

A recent profile of Dr. Morris Chang of General Instrument Corp., [ElectronicsWeek, *Sept. 3, 1984, p. 53*] *incorrectly identified him in the caption; he is the firm's chief operating officer. General Instrument's holding in United Satellite Communications Inc. was incorrectly stated; it is 12% of the company's stock.*

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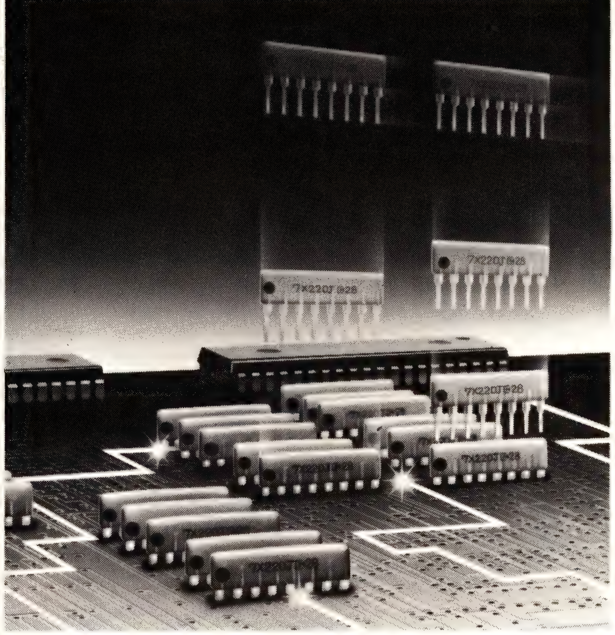

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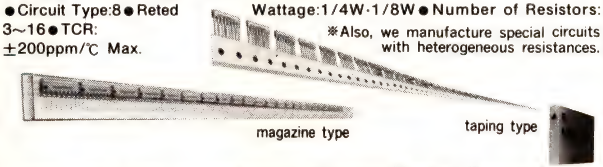

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- ■ For more information of complete product line see advertisement in the latest Electronics Buyers Guide
- * Advertisers in Electronics International
- ‡ Advertisers in Electronics domestic edition
- ☐ Advertisers in regional issue

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ANOTHER FLANKING MOVEMENT IN JAPAN

Imagine IBM, Burroughs, Texas Instruments, and Wang going to the FCC and asking for approval to set up an exclusive organization to certify all telecommunications equipment in the U.S. market, with financing from Morgan Guaranty and Bank of America." That is how an adviser to the U.S. Embassy in Tokyo portrays Japan's latest end run around its own open-market laws.

This time it's telecommunications, a market supposed to open wider to foreigners next April. A key is the standards and certification system, and that's where the Japanese appear to be doing their utmost to quietly erect new barriers—in this case an agency consisting only of Japanese telecommunications houses with the cooperation of Nippon Telegraph & Telephone Public Corp. with the whole affair financed by Japanese banks (see p. 29).

But why should anyone be surprised? The Japanese are nothing if not consistent in their singleminded pursuit of worldwide high-technology hegemony, and they have been working at it with striking success for decades now. When the rest of the world gets wise to their game, they simply change strategy. What *is* surprising is that any smart company managers would expect their opposite numbers in Japan to permit competition in the home islands on an even footing.

The next question is, what should be done? With little time left to do anything, a trade delegation from the U.S. arrived in Tokyo a few days ago; the brewing telecommunications war is certain to be a topic of whatever discussions take place.

Meanwhile, it would behoove chief executives of U.S. companies that want to compete in Japan to keep their eyes on the real bottom line of such activity: when the Japanese say they are going to permit competition, that's the time to start looking for loopholes.

THE HIDDEN PENALTY IN JOINT VENTURES

One of the new Japanese strategies in the trade wars is the joint venture. To get around such walls as the "voluntary" auto-export limit forced on them by the U.S., they simply set up a manufacturing facility in the U.S. in partnership with a domestic maker, thereby ensuring that all is strictly according to Hoyle. But those arrangements represent for the most part nothing less than a theft of U.S. technological know-how.

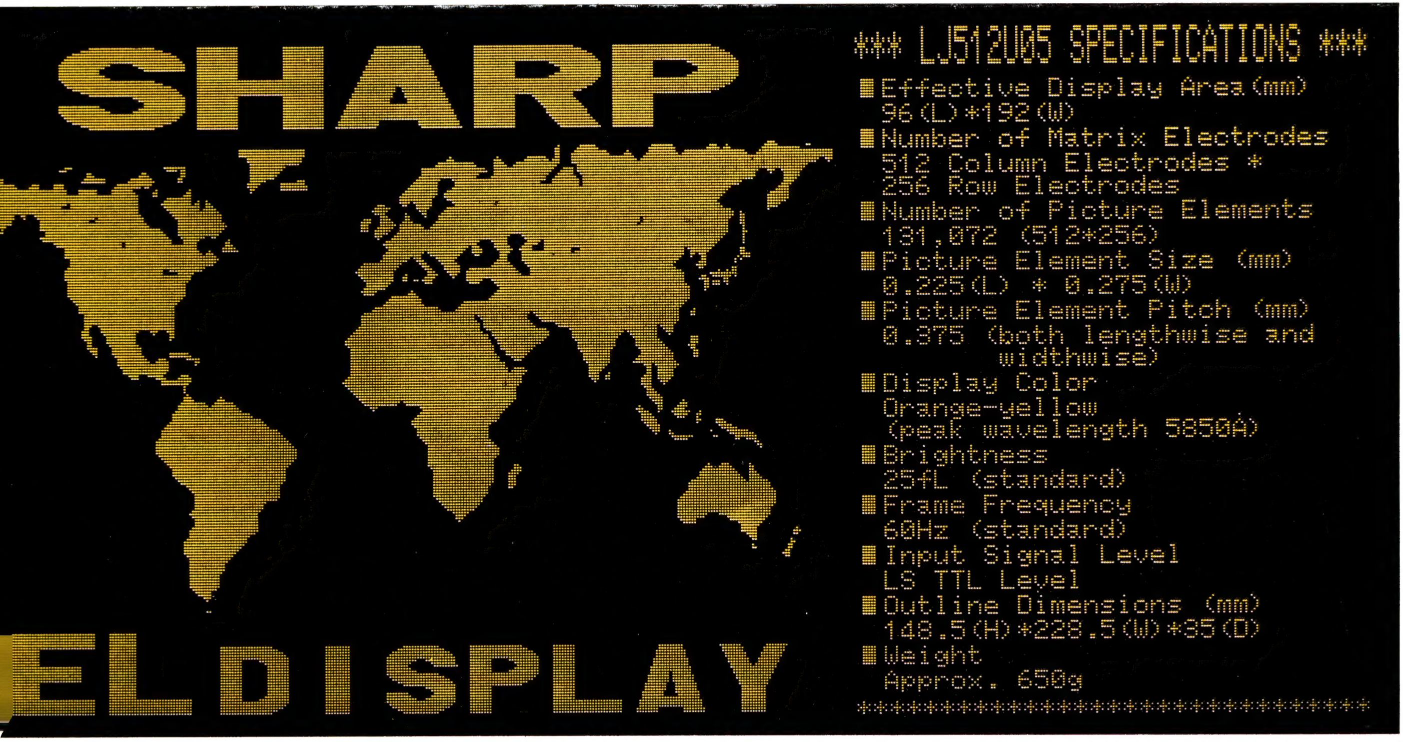
Typically, the research and development is done in the U.S. Then the results are transferred to Japan, where most of the manufacturing—usually automated—is done. This gives the Japanese the opportunity to hone their robotics skills. Finally, what the American plant gets to do is assemble the product: the low-tech part of the operation.

This approach represents nothing less than a mortgage on America's technological future for next quarter's results. This country would be left with the low end of the production cycle, plus research and development whose fruits would feed the Japanese. Those joint manufacturing ventures could wind up being a mistake in the long run.

25 LINES OF 80 CHARACTERS!

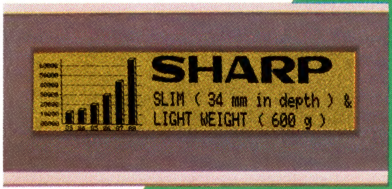
LAT PANEL DISPLAYS AVAILABLE NOW!!

This is the actual effective display size of LJ512U05

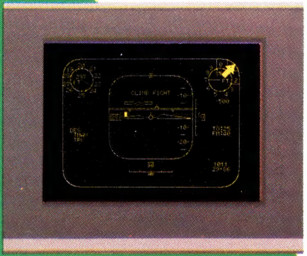


```
*** LJ512U05 SPECIFICATIONS ***
■Effective Display Area(mm)
 96(L)*192(W)
■Number of Matrix Electrodes
 512 Column Electrodes *
 256 Row Electrodes
■Number of Picture Elements
 131,072 (512*256)
■Picture Element Size (mm)
 0.225(L) * 0.275(W)
■Picture Element Pitch (mm)
 0.375 (both lengthwise and
        widthwise)
■Display Color
 Orange-yellow
 (peak wavelength 5850Å)
■Brightness
 25fL (standard)
■Frame Frequency
 60Hz (standard)
■Input Signal Level
 LS TTL Level
■Outline Dimensions (mm)
 148.5(H)*228.5(W)*35(D)
■Weight
 Approx. 650g
*********************************
```

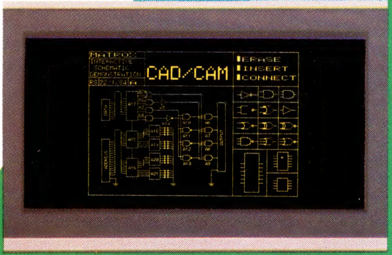
)'s full line of EL (Electro Luminescent) Displays are thin
m), lightweight (650 grams), low power (15 watts max)
ne two latest editions can display 25 lines of 80 char-
;. These "State of The Art" Displays feature; line by
crolling, blinking characters, full graphics and a simple 4 line interface. EL's bright, crisp, easy to read characters will enhance the marketability of any product. Design the leading edge of display technology into your products today using displays from Sharp, the world's largest manufacturer of EL Displays!



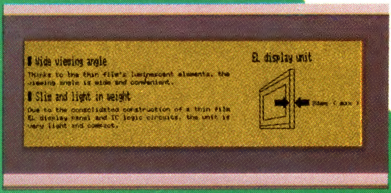
U01 • Ideal for written
ers • Effective display area
ı×179 2mm • Number of picture
ts 512×128
e Dimensions (mm): 108.5(H) ×
) × 34(D)



LJ 320U01 • Ideal for fine graphics as well as written characters • Effective display area 90mm × 120mm • Number of picture elements 320×240 • Outline Dimensions (mm): 148.5(H) × 178.5(W) × 34(D)



U05 • Ideal for fine graphics as
written characters • Effective
area 96mm × 192mm • Number
re elements 512×256
e Dimensions (mm): 148.5(H) ×
) × 34(D)



■ Wide viewing angle

Thanks to the thin film's luminescent elements, the viewing angle is wide and convenient.

■ Slim and light in weight

Due to the consolidated construction of a thin film EL display panel and IC logic circuits, the unit is very light and compact.

LJ 640U01 • Ideal for written characters • Effective display area 60mm × 192mm • Number of picture elements 640×200 • Outline Dimensions (mm): 108.5(H) × 228.5(W) × 34(D)

EL DISPLAY

SHARP

SHARP CORPORATION, JAPAN

SHARP CORPORATION **International Business Group, Electronic Components Sales Dept.**
22-22, Nagaike-cho, Abeno-ku, Osaka 545, JAPAN
Tel: (06) 621-1221 Cable: LABOMET OSAKA Telex: J63428 Attn: OSKPA (LABOMET A-D)

U.S.A.: SHARP ELECTRONICS CORPORATION
10 Sharp Plaza, Paramus, New Jersey 07652 Tel: (201) 265-5600
Electronic Components Dept.

EUROPE: SHARP ELECTRONICS (EUROPE) GMBH
Sonninstrasse 3, 2000 Hamburg 1, F.R. Germany Tel: (040) 23775—1
Electronic Components Dept.

Circle 901 on reader service card

UDS for DDS?

YES!

Getting ready to take advantage of digital data service (DDS)? Then you'll want a DSU/CSU from a company that's already a leader in the conventional modem business.

Universal Data Systems now offers the DDS-56 and the DDS-9.6 for access to the DDS network at 56 kbps and 9.6 kbps respectively. Each combines DSU and CSU in a single package. They are FCC certified for connection to the DDS network and are direct replacements for Bell units.

Both UDS devices offer built-in diagnostics, WECO compatibility, automatic line equalization and unattended remote loopback capability. Built-in interfaces are CCITT V.35 for the DDS-56 and RS-232C for the DDS-9.6.

For prices and complete specifications contact Universal Data Systems, 5000 Bradford Drive, Huntsville, AL 35805. Phone 205/837-8100; Telex 752602 UDS HTV.

Universal Data Systems
MOTOROLA INC.
Information Systems Group

Inquiry Hotline: 800/633-2252, Ext. 363

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Circle 902 on reader service card

Created by Dayner/Hall, Inc., Winter Park, Florid